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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

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Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	143
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl250v5-cs196i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Flash Advantages

Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system powerup (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based IGLOO devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and

Combinatorial Cells Contribution—P_{C-CELL}

 $\mathsf{P}_{\text{C-CELL}} = \mathsf{N}_{\text{C-CELL}} * \alpha_1 / 2 * \mathsf{P}_{\text{AC7}} * \mathsf{F}_{\text{CLK}}$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

 F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

 $\mathsf{P}_{\mathsf{NET}} = (\mathsf{N}_{\mathsf{S}\text{-}\mathsf{CELL}} + \mathsf{N}_{\mathsf{C}\text{-}\mathsf{CELL}}) * \alpha_1 / 2 * \mathsf{P}_{\mathsf{AC8}} * \mathsf{F}_{\mathsf{CLK}}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

 $N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

 F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

 $P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

 $N_{\mbox{\rm INPUTS}}$ is the number of I/O input buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—P_{OUTPUTS}

 $P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

 $N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

 β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

 $P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$

 $N_{\mbox{\scriptsize BLOCKS}}$ is the number of RAM blocks used in the design.

F_{READ-CLOCK} is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations.

F_{WRITE-CLOCK} is the memory write clock frequency.

 β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution—P_{PLL}

 $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[†]

[†] If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (P_{AC13}* F_{CLKOUT} product) to the total PLL contribution.

User I/O Characteristics

Timing Model



Figure 2-3 • Timing Model

Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J = 70^{\circ}$ C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Table 2-35 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-CaseConditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	tpour (ns)	t _{DP} (ns)	t _{DIN} (ns)	t _{PY} (ns)	t _{EOUT} (ns)	t _{ZL} (ns)	t _{ZH} (ns)	t _{LZ} (ns)	t _{HZ} (ns)	t _{ZLS} (ns)	t _{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	_	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3 V LVCMOS Wide Range ²	100 µA	12	High	5	_	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5 V LVCMOS	12 mA	12	High	5		1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8 V LVCMOS	8 mA	8	High	5	_	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5 V LVCMOS	4 mA	4	High	5	_	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2 V LVCMOS	2 mA	2	High	5	_	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2 V LVCMOS Wide Range ³	100 μA	2	High	5	-	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3 V PCI	Per PCI spec	_	High	10	25 ²	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3 V PCI-X	Per PCI-X spec	_	High	10	25 ²	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Notes:

 The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification

4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.

5. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		V _{OL}	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Table 2-49 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Test Point
Datapath
$$\downarrow$$
 5 pF $R = 1 k$
Enable Path \downarrow $R = 1 k$
 $Test Point$
Enable Path \downarrow $Test Point$
 $F = 1 k$
 $R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}$
 $R to GND for t_{HZ} / t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}$

Figure 2-7 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-77 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: TJ = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case VCCI = 2.7
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t _{dout}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
100 µA	2 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	4 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	6 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns
100 µA	8 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 μA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-78 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t _{dout}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
100 µA	2 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	4 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	6 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
100 µA	8 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 μA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	v	1L	v	IH	VOL	VОН	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Table 2-79 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

 Table 2-80 •
 Minimum and Maximum DC Input and Output Levels

 Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	.5 V VCMOS VIL rive Min Max		v	ΊH	VOL	vон	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Table 2-104 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Standard Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	2.62	0.18	0.98	0.66	2.67	2.59	1.67	1.29	2.62	ns
4 mA	Std.	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	2.18	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-105 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	6.97	0.26	1.11	1.10	7.08	6.48	2.87	2.29	12.87	12.27	ns
4 mA	Std.	1.55	5.91	0.26	1.11	1.10	6.01	5.57	3.21	3.14	11.79	11.36	ns
6 mA	Std.	1.55	5.16	0.26	1.11	1.10	5.24	4.95	3.45	3.55	11.03	10.74	ns
8 mA	Std.	1.55	4.90	0.26	1.11	1.10	4.98	4.81	3.50	3.66	10.77	10.60	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-106 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.86	2.34	9.49	9.51	ns
4 mA	Std.	1.55	3.12	0.26	1.11	1.10	3.16	2.97	3.21	3.22	8.95	8.75	ns
6 mA	Std.	1.55	2.79	0.26	1.11	1.10	2.83	2.59	3.45	3.65	8.62	8.38	ns
8 mA	Std.	1.55	2.73	0.26	1.11	1.10	2.77	2.52	3.50	3.75	8.56	8.30	ns
12 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
16 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-138 • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range	
Applicable to Standard Plus I/O Banks	

1.2 V LVCI Wide Rang	MOS ge		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁴	Max. mA ⁴	μΑ ⁵	μA ⁵
100 µA	2mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 μA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4. Currents are measured at 100°C junction temperature and maximum voltage.

5. Currents are measured at 85°C junction temperature.

6. Software default selection highlighted in gray.

Table 2-139 • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard I/O Banks

1.2 V LVCI Wide Rang	MOS ge		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 µA	1 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

 The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 μA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4. Currents are measured at 100°C junction temperature and maximum voltage.

5. Currents are measured at 85°C junction temperature.

6. Software default selection highlighted in gray.

Table 2-140 • 1.2 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-75 for worst-case timing.

DC Parameter	Description	Min.	Тур.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ²	Input High Leakage Current			10	μΑ
IIL ²	Input Low Leakage Current			10	μΑ
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF ⁴	Input Differential Voltage	100	350		mV

Table 2-147 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IOL/IOH is defined by VODIFF/(resistor network)

2. Currents are measured at 85°C junction temperature.

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: **Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-149 • LVDS – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-150 • LVDS – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	1.55	2.19	0.25	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-159 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
tOSUD	Data Setup Time for the Output Data Register	0.51	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t _{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
tOWPRE	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-160 • Output Data Register Propagation Delays Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
tOSUD	Data Setup Time for the Output Data Register	1.15	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	ns
tOSUE	Enable Setup Time for the Output Data Register	1.11	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.



Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t _{DDRICLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t _{DDRICLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t _{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t _{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t _{DDRIHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t _{DDRIHD2}	Data Hold for Input DDR (posedge)	0.00	ns
t _{DDRICLR2Q1}	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
t _{DDRICLR2Q2}	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
t _{DDRIREMCLR}	Asynchronous Clear Removal Time for Input DDR	0.00	ns
t _{DDRIRECCLR}	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t _{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
t _{DDRICKMPWH}	Clock Minimum Pulse Width High for Input DDR	0.31	ns
t _{DDRICKMPWL}	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F _{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.



Figure 2-34 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.



Figure 2-35 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.

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IGLOO Low Power Flash FPGAs

QN132			QN132	QN132			
Pin Number	AGL060 Function	Pin Number	AGL060 Function	Pin Number	AGL060 Function		
A1	GAB2/IO00RSB1	A37	GBB1/IO25RSB0	B24	GDC0/IO49RSB0		
A2	IO93RSB1	A38	GBC0/IO22RSB0	B25	GND		
A3	VCCIB1	A39	VCCIB0	B26	NC		
A4	GFC1/IO89RSB1	A40	IO21RSB0	B27	GCB2/IO45RSB0		
A5	GFB0/IO86RSB1	A41	IO18RSB0	B28	GND		
A6	VCCPLF	A42	IO15RSB0	B29	GCB0/IO41RSB0		
A7	GFA1/IO84RSB1	A43	IO14RSB0	B30	GCC1/IO38RSB0		
A8	GFC2/IO81RSB1	A44	IO11RSB0	B31	GND		
A9	IO78RSB1	A45	GAB1/IO08RSB0	B32	GBB2/IO30RSB0		
A10	VCC	A46	NC	B33	VMV0		
A11	GEB1/IO75RSB1	A47	GAB0/IO07RSB0	B34	GBA0/IO26RSB0		
A12	GEA0/IO72RSB1	A48	IO04RSB0	B35	GBC1/IO23RSB0		
A13	GEC2/IO69RSB1	B1	IO01RSB1	B36	GND		
A14	IO65RSB1	B2	GAC2/IO94RSB1	B37	IO20RSB0		
A15	VCC	B3	GND	B38	IO17RSB0		
A16	IO64RSB1	B4	GFC0/IO88RSB1	B39	GND		
A17	IO63RSB1	B5	VCOMPLF	B40	IO12RSB0		
A18	IO62RSB1	B6	GND	B41	GAC0/IO09RSB0		
A19	IO61RSB1	B7	GFB2/IO82RSB1	B42	GND		
A20	IO58RSB1	B8	IO79RSB1	B43	GAA1/IO06RSB0		
A21	GDB2/IO55RSB1	B9	GND	B44	GNDQ		
A22	NC	B10	GEB0/IO74RSB1	C1	GAA2/IO02RSB1		
A23	GDA2/IO54RSB1	B11	VMV1	C2	IO95RSB1		
A24	TDI	B12	FF/GEB2/IO70RSB	C3	VCC		
A25	TRST		1	C4	GFB1/IO87RSB1		
A26	GDC1/IO48RSB0	B13	IO67RSB1	C5	GFA0/IO85RSB1		
A27	VCC	B14	GND	C6	GFA2/IO83RSB1		
A28	IO47RSB0	B15	NC	C7	IO80RSB1		
A29	GCC2/IO46RSB0	B16	NC	C8	VCCIB1		
A30	GCA2/IO44RSB0	B17	GND	C9	GEA1/IO73RSB1		
A31	GCA0/IO43RSB0	B18	IO59RSB1	C10	GNDQ		
A32	GCB1/IO40RSB0	B19	GDC2/IO56RSB1	C11	GEA2/IO71RSB1		
A33	IO36RSB0	B20	GND	C12	IO68RSB1		
A34	VCC	B21	GNDQ	C13	VCCIB1		
A35	IO31RSB0	B22	TMS	C14	NC		
A36		B23	TDO	C15	NC		

Microsemi

Package Pin Assignments

FG144				
Pin Number	AGL250 Function			
K1	GEB0/IO99NDB3			
K2	GEA1/IO98PDB3			
K3	GEA0/IO98NDB3			
K4	GEA2/IO97RSB2			
K5	IO90RSB2			
K6	IO84RSB2			
K7	GND			
K8	IO66RSB2			
K9	GDC2/IO63RSB2			
K10	GND			
K11	GDA0/IO60VDB1			
K12	GDB0/IO59VDB1			
L1	GND			
L2	VMV3			
L3	FF/GEB2/IO96RSB2			
L4	IO91RSB2			
L5	VCCIB2			
L6	IO82RSB2			
L7	IO80RSB2			
L8	IO72RSB2			
L9	TMS			
L10	VJTAG			
L11	VMV2			
L12	TRST			
M1	GNDQ			
M2	GEC2/IO95RSB2			
M3	IO92RSB2			
M4	IO89RSB2			
M5	IO87RSB2			
M6	IO85RSB2			
M7	IO78RSB2			
M8	IO76RSB2			
M9	TDI			
M10	VCCIB2			
M11	VPUMP			
M12	GNDQ			



Package Pin Assignments

FG484		
Pin Number	AGL400 Function	
E13	IO38RSB0	
E14	IO42RSB0	
E15	GBC1/IO55RSB0	
E16	GBB0/IO56RSB0	
E17	IO44RSB0	
E18	GBA2/IO60PDB1	
E19	IO60NDB1	
E20	GND	
E21	NC	
E22	NC	
F1	NC	
F2	NC	
F3	NC	
F4	IO154VDB3	
F5	IO155VDB3	
F6	IO11RSB0	
F7	IO07RSB0	
F8	GAC0/IO04RSB0	
F9	GAC1/IO05RSB0	
F10	IO20RSB0	
F11	IO24RSB0	
F12	IO33RSB0	
F13	IO39RSB0	
F14	IO45RSB0	
F15	GBC0/IO54RSB0	
F16	IO48RSB0	
F17	VMV0	
F18	IO61NPB1	
F19	IO63PDB1	
F20	NC	
F21	NC	
F22	NC	
G1	NC	
G2	NC	
G3	NC	
G4	IO151VDB3	

FG484		
Pin Number	AGL600 Function	
G5	IO171PDB3	
G6	GAC2/IO172PDB3	
G7	IO06RSB0	
G8	GNDQ	
G9	IO10RSB0	
G10	IO19RSB0	
G11	IO26RSB0	
G12	IO30RSB0	
G13	IO40RSB0	
G14	IO45RSB0	
G15	GNDQ	
G16	IO50RSB0	
G17	GBB2/IO61PPB1	
G18	IO53RSB0	
G19	IO63NDB1	
G20	NC	
G21	NC	
G22	NC	
H1	NC	
H2	NC	
H3	VCC	
H4	IO166PDB3	
H5	IO167NPB3	
H6	IO172NDB3	
H7	IO169NDB3	
H8	VMV0	
H9	VCCIB0	
H10	VCCIB0	
H11	IO25RSB0	
H12	IO31RSB0	
H13	VCCIB0	
H14	VCCIB0	
H15	VMV1	
H16	GBC2/IO62PDB1	
H17	IO67PPB1	
H18	IO64PPB1	

FG484		
Pin Number	AGL600 Function	
K11	GND	
K12	GND	
K13	GND	
K14	VCC	
K15	VCCIB1	
K16	GCC1/IO69PPB1	
K17	IO65NPB1	
K18	IO75PDB1	
K19	IO75NDB1	
K20	NC	
K21	IO76NDB1	
K22	IO76PDB1	
L1	NC	
L2	IO155PDB3	
L3	NC	
L4	GFB0/IO163NPB3	
L5	GFA0/IO162NDB3	
L6	GFB1/IO163PPB3	
L7	VCOMPLF	
L8	GFC0/IO164NPB3	
L9	VCC	
L10	GND	
L11	GND	
L12	GND	
L13	GND	
L14	VCC	
L15	GCC0/IO69NPB1	
L16	GCB1/IO70PPB1	
L17	GCA0/IO71NPB1	
L18	IO67NPB1	
L19	GCB0/IO70NPB1	
L20	IO77PDB1	
L21	IO77NDB1	
L22	IO78NPB1	
M1	NC	
M2	IO155NDB3	

FG484		
Pin Number	AGL1000 Function	
B7	IO15RSB0	
B8	IO19RSB0	
B9	IO24RSB0	
B10	IO31RSB0	
B11	IO39RSB0	
B12	IO48RSB0	
B13	IO54RSB0	
B14	IO58RSB0	
B15	IO63RSB0	
B16	IO66RSB0	
B17	IO68RSB0	
B18	IO70RSB0	
B19	NC	
B20	NC	
B21	VCCIB1	
B22	GND	
C1	VCCIB3	
C2	IO220PDB3	
C3	NC	
C4	NC	
C5	GND	
C6	IO10RSB0	
C7	IO14RSB0	
C8	VCC	
C9	VCC	
C10	IO30RSB0	
C11	IO37RSB0	
C12	IO43RSB0	
C13	NC	
C14	VCC	
C15	VCC	
C16	NC	
C17	NC	
C18	GND	
C19	NC	
C20	NC	

IGLOO Low Power Flash FPGAs

Revision / Version	Changes	Page
DC & Switching, cont'd.	Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.	2-39
Revision 9 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change $1.2 \text{ V} / 1.5 \text{ V}$ to 1.2 V to 1.5 V .	N/A
Revision 8 (Jun 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change $1.2 \text{ V} / 1.5 \text{ V}$ to 1.2 V to 1.5 V .	N/A
DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time.	N/A
	The power data table has been updated to match SmartPower data rather then simulation values. AGL015 global clock delays have been added.	
	Table 2-1 • Absolute Maximum Ratings was updated to combine the VCCI and VMV parameters in one row. The word "output" from the parameter description for VCCI and VMV, and table note 3 was added.	2-1
	Table 2-2 • Recommended Operating Conditions 1 was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the VCCI parameter row, and table note 9 was added.	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-3
	VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new.	2-5
	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode*, Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*, and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode1 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-9