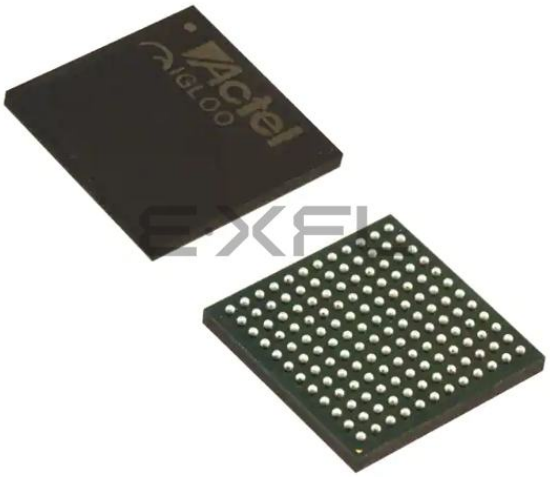

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl250v5-fgg144

Figure 1-5 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-2 • **Recommended Operating Conditions** [1]

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature [2]		0 to +85	–40 to +100	°C
VCC[3]	1.5 V DC core supply voltage[5]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core supply voltage [4,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[5]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage[4,6]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [9]	1.2 V DC core supply voltage[6]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range DC supply voltage[6]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-24. VCCI should be at the same voltage within a given I/O bank.*
4. *All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
5. *For IGLOO® V5 devices*
6. *For IGLOO V2 devices only, operating at VCCI ≥ VCC.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
9. *VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information.*
10. *3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.*

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC®3* and *ProASIC3E* FPGA fabric user guides for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

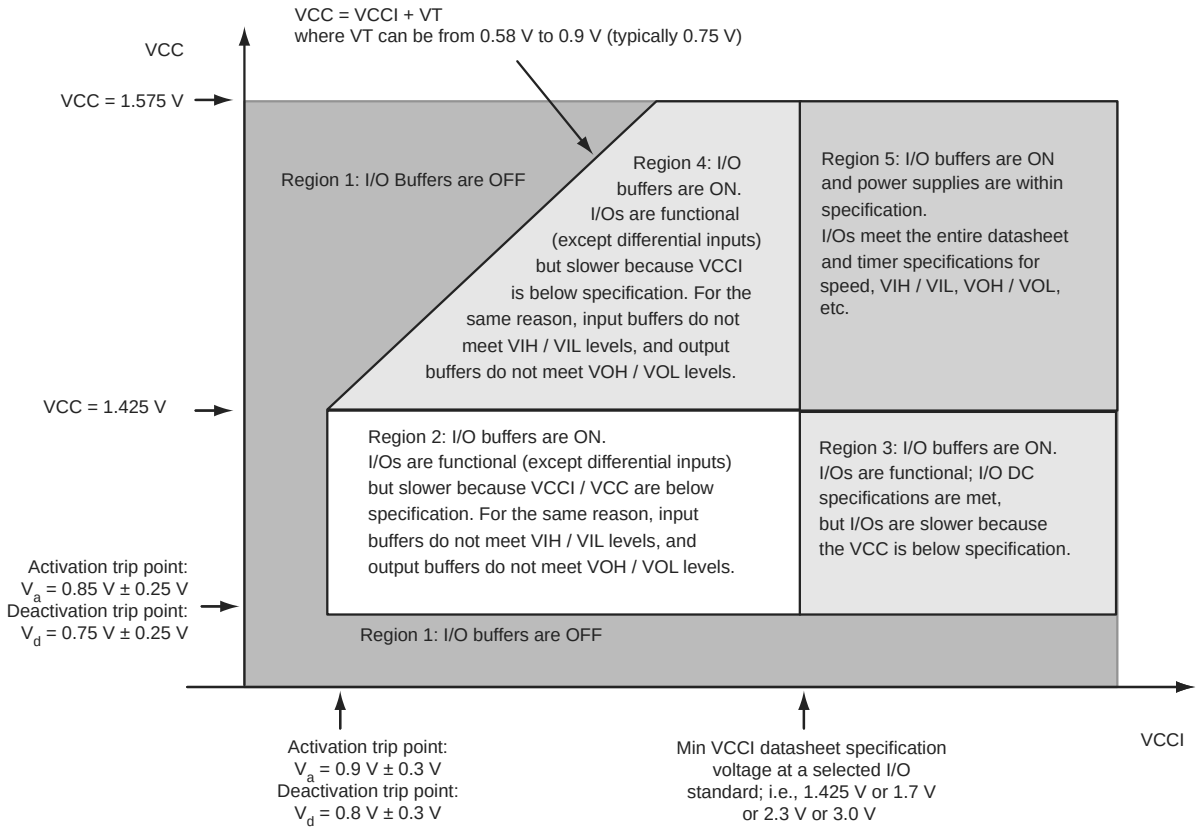


Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.†

† *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-28 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	IIL[4]	IIH[5]	IIL[4]	IIH[5]
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[3]	10	10	15	15
1.2 V LVCMOS Wide Range[3]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
5. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

Table 2-69 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	4 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	6 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	8 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	12 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns
100 µA	16 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-70 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	4 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	6 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	8 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	12 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
100 µA	16 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

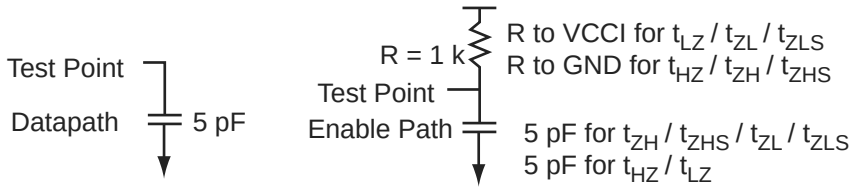


Figure 2-11 • **AC Loading**

Table 2-130 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-131 • **1.2 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-132 • **1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-133 • **1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-134 • **1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14. The input and output buffer delays are available in the LVDS section in Table 2-149 on page 2-81 and Table 2-150 on page 2-81.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

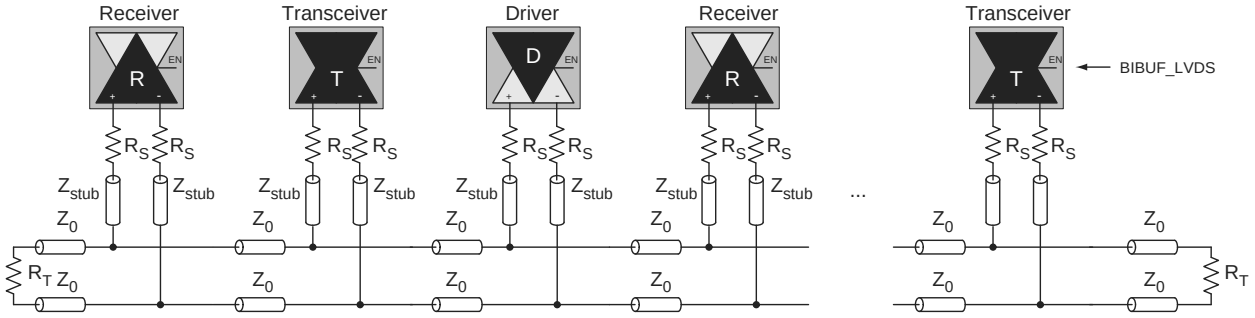


Figure 2-14 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

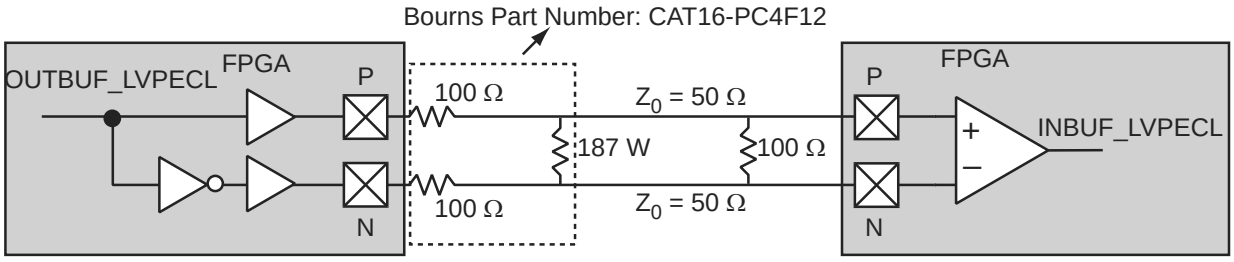


Figure 2-15 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-156 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-17 on page 2-86 for more information.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

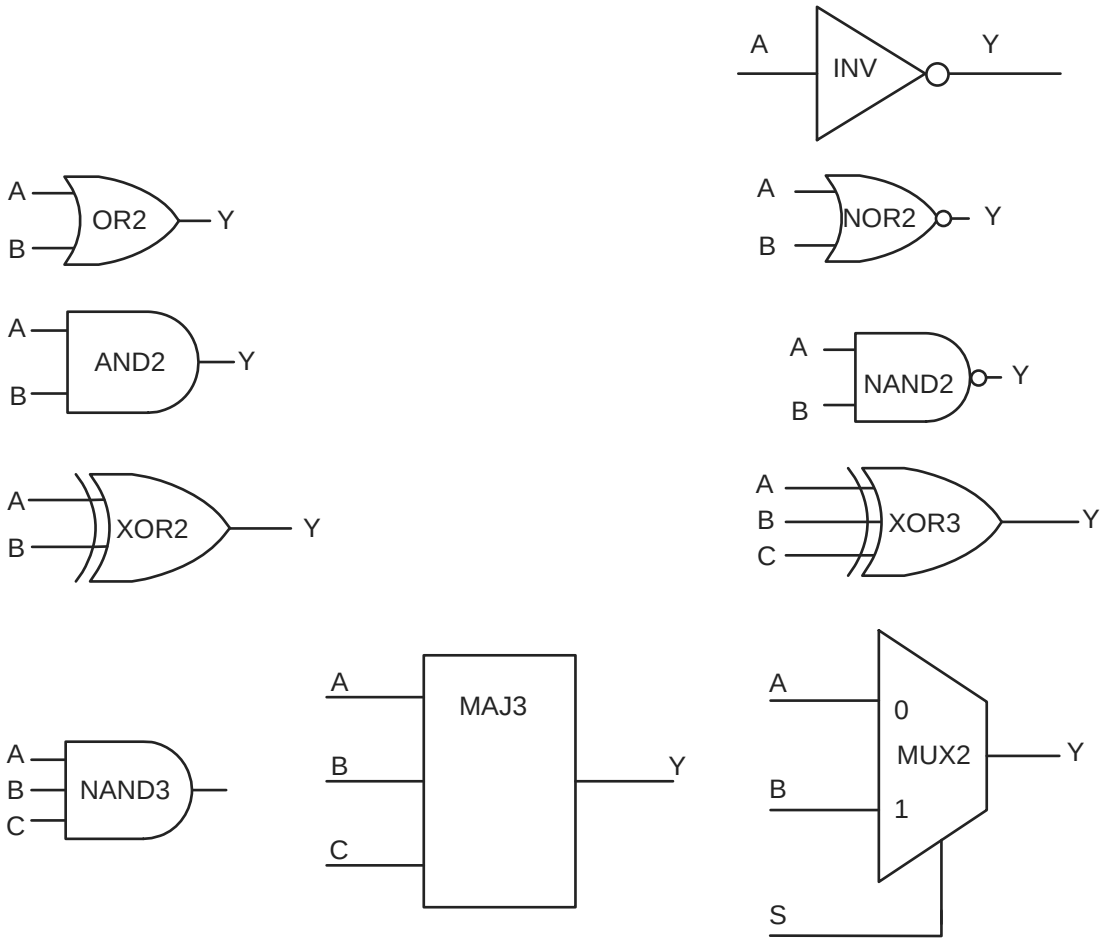


Figure 2-25 • **Sample of Combinatorial Cells**

Global Resource Characteristics

AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 2-29 is an example of a global tree used for clock routing. The global tree presented in Figure 2-29 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

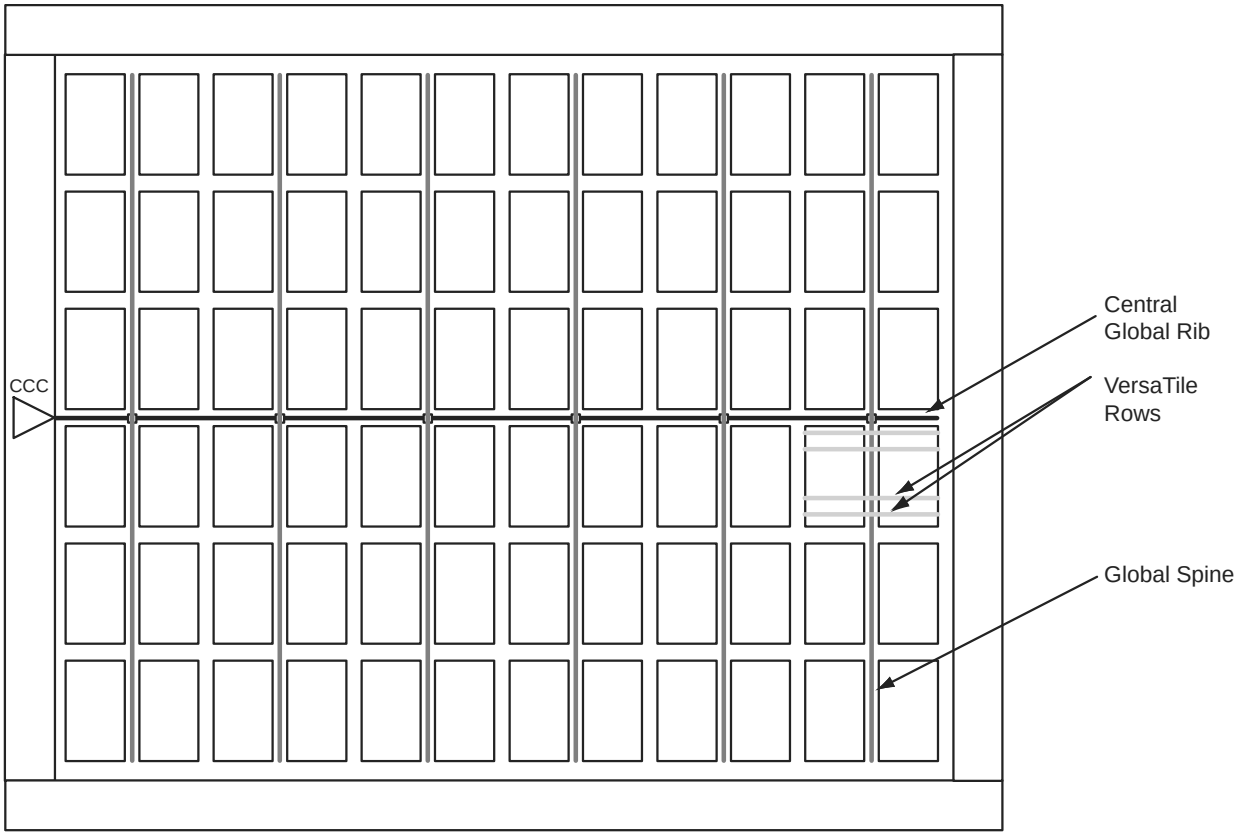


Figure 2-29 • **Example of Global Tree Use in an AGL250 Device for Clock Routing**

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-189 • IGLOO CCC/PLL Specification
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

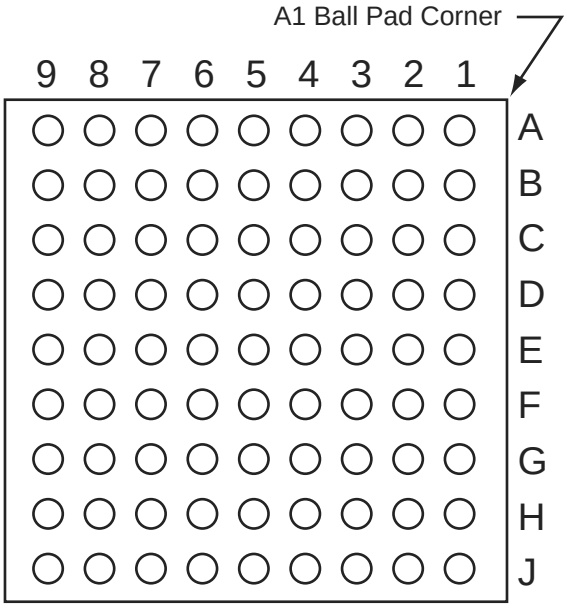
Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4, 5]			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7]			
	SSO ≥ 4[8]	SSO ≥ 8[8]	SSO ≥ 16[8]	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *The AGL030 device does not support a PLL.*
5. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.*

4 – Package Pin Assignments

UC81

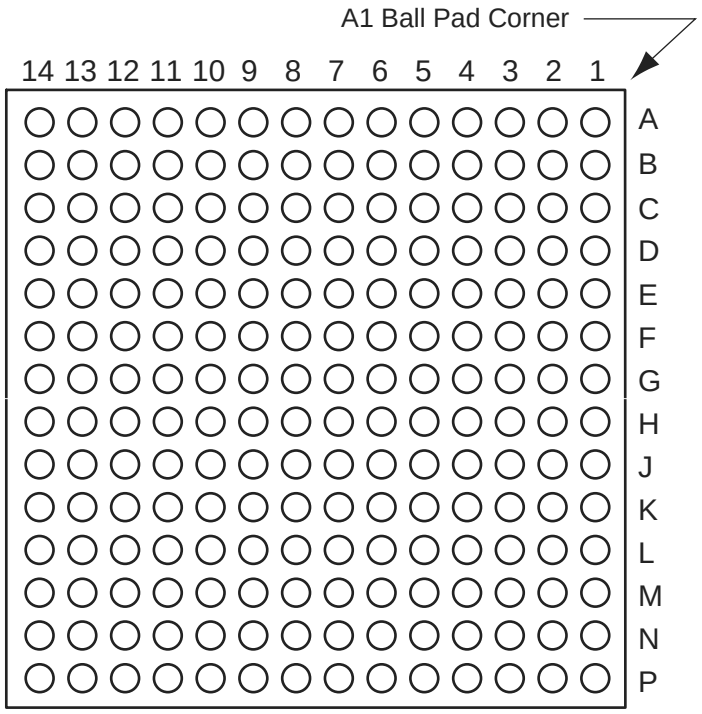


Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS196



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN132	
Pin Number	**AGL060 Function**
A1	GAB2/IO00RSB1
A2	IO93RSB1
A3	VCCIB1
A4	GFC1/IO89RSB1
A5	GFB0/IO86RSB1
A6	VCCPLF
A7	GFA1/IO84RSB1
A8	GFC2/IO81RSB1
A9	IO78RSB1
A10	VCC
A11	GEB1/IO75RSB1
A12	GEA0/IO72RSB1
A13	GEC2/IO69RSB1
A14	IO65RSB1
A15	VCC
A16	IO64RSB1
A17	IO63RSB1
A18	IO62RSB1
A19	IO61RSB1
A20	IO58RSB1
A21	GDB2/IO55RSB1
A22	NC
A23	GDA2/IO54RSB1
A24	TDI
A25	TRST
A26	GDC1/IO48RSB0
A27	VCC
A28	IO47RSB0
A29	GCC2/IO46RSB0
A30	GCA2/IO44RSB0
A31	GCA0/IO43RSB0
A32	GCB1/IO40RSB0
A33	IO36RSB0
A34	VCC
A35	IO31RSB0
A36	GBA2/IO28RSB0

QN132	
Pin Number	**AGL060 Function**
A37	GBB1/IO25RSB0
A38	GBC0/IO22RSB0
A39	VCCIB0
A40	IO21RSB0
A41	IO18RSB0
A42	IO15RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	GAB1/IO08RSB0
A46	NC
A47	GAB0/IO07RSB0
A48	IO04RSB0
B1	IO01RSB1
B2	GAC2/IO94RSB1
B3	GND
B4	GFC0/IO88RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO82RSB1
B8	IO79RSB1
B9	GND
B10	GEB0/IO74RSB1
B11	VMV1
B12	FF/GEB2/IO70RSB1
B13	IO67RSB1
B14	GND
B15	NC
B16	NC
B17	GND
B18	IO59RSB1
B19	GDC2/IO56RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO

QN132	
Pin Number	**AGL060 Function**
B24	GDC0/IO49RSB0
B25	GND
B26	NC
B27	GCB2/IO45RSB0
B28	GND
B29	GCB0/IO41RSB0
B30	GCC1/IO38RSB0
B31	GND
B32	GBB2/IO30RSB0
B33	VMV0
B34	GBA0/IO26RSB0
B35	GBC1/IO23RSB0
B36	GND
B37	IO20RSB0
B38	IO17RSB0
B39	GND
B40	IO12RSB0
B41	GAC0/IO09RSB0
B42	GND
B43	GAA1/IO06RSB0
B44	GNDQ
C1	GAA2/IO02RSB1
C2	IO95RSB1
C3	VCC
C4	GFB1/IO87RSB1
C5	GFA0/IO85RSB1
C6	GFA2/IO83RSB1
C7	IO80RSB1
C8	VCCIB1
C9	GEA1/IO73RSB1
C10	GNDQ
C11	GEA2/IO71RSB1
C12	IO68RSB1
C13	VCCIB1
C14	NC
C15	NC

VQ100	
Pin Number	**AGL250 Function**
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	**AGL250 Function**
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	**AGL250 Function**
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

FG484	
Pin Number	**AGL400 Function**
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2

FG484	
Pin Number	**AGL1000 Function**
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	**AGL1000 Function**
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2

Revision	Changes	Page
Revision 23 (December 2012)	The "IGLOO Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43173).	III
	The note in Table 2-189 · IGLOO CCC/PLL Specification and Table 2-190 · IGLOO CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42564). Additionally, note regarding SSOs was added.	2-115, 2-116
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 22 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40271).	N/A
Revision 21 (May 2012)	Under AGL125, in the Package Pin list, CS121 was incorrectly added to the datasheet in revision 19 and has been removed (SAR 38217).	I to IV
	Corrected the inadvertent error for Max Values for LVPECL VIH and revised the same to '3.6' in Table 2-151 · Minimum and Maximum DC Input and Output Levels (SAR 37685).	2-82
	Figure 2-38 • FIFO Read and Figure 2-39 • FIFO Write have been added (SAR 34841).	2-127
	The following sentence was removed from the VMVx description in the "Pin Descriptions" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38317). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1