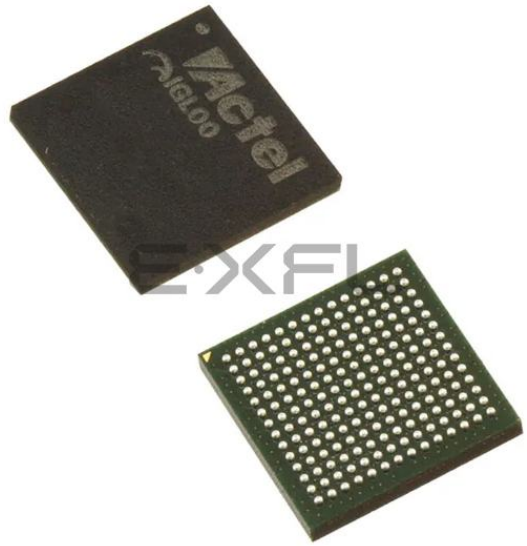

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	9216
Total RAM Bits	55296
Number of I/O	143
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl400v2-cs196

Table 2-2 • **Recommended Operating Conditions** [1]

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature [2]		0 to +85	–40 to +100	°C
VCC[3]	1.5 V DC core supply voltage[5]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core supply voltage [4,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[5]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage[4,6]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [9]	1.2 V DC core supply voltage[6]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range DC supply voltage[6]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-24. VCCI should be at the same voltage within a given I/O bank.*
4. *All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
5. *For IGLOO® V5 devices*
6. *For IGLOO V2 devices only, operating at VCCI ≥ VCC.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
9. *VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information.*
10. *3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.*

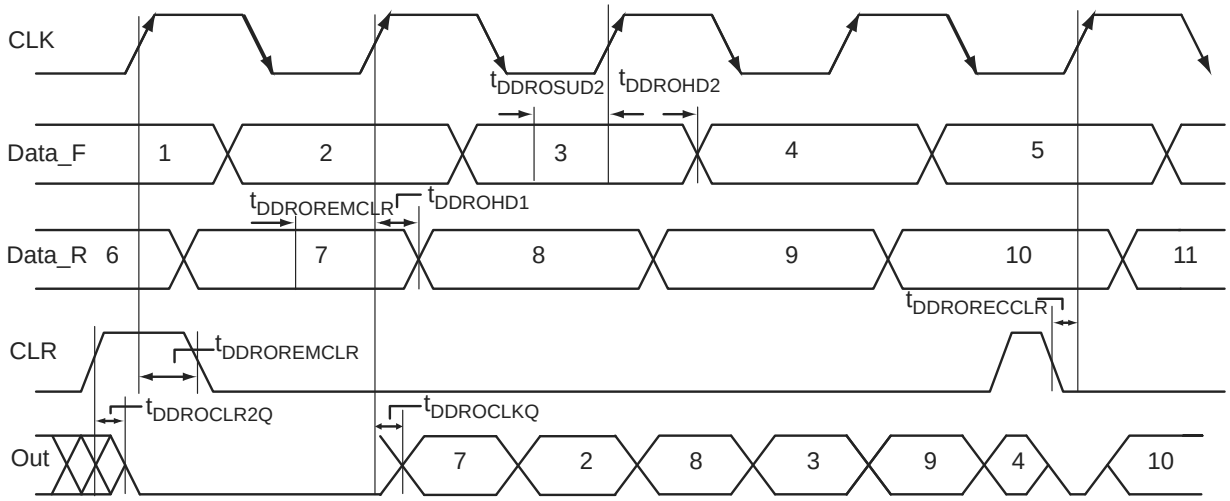


Figure 2-24 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-167 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

***Table 2-172* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-175 • **AGL060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-176 • **AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-189 • IGLOO CCC/PLL Specification
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4, 5]			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7]			
	SSO ≥ 4[8]	SSO ≥ 8[8]	SSO ≥ 16[8]	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *The AGL030 device does not support a PLL.*
5. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.*

1.2 V DC Core Voltage

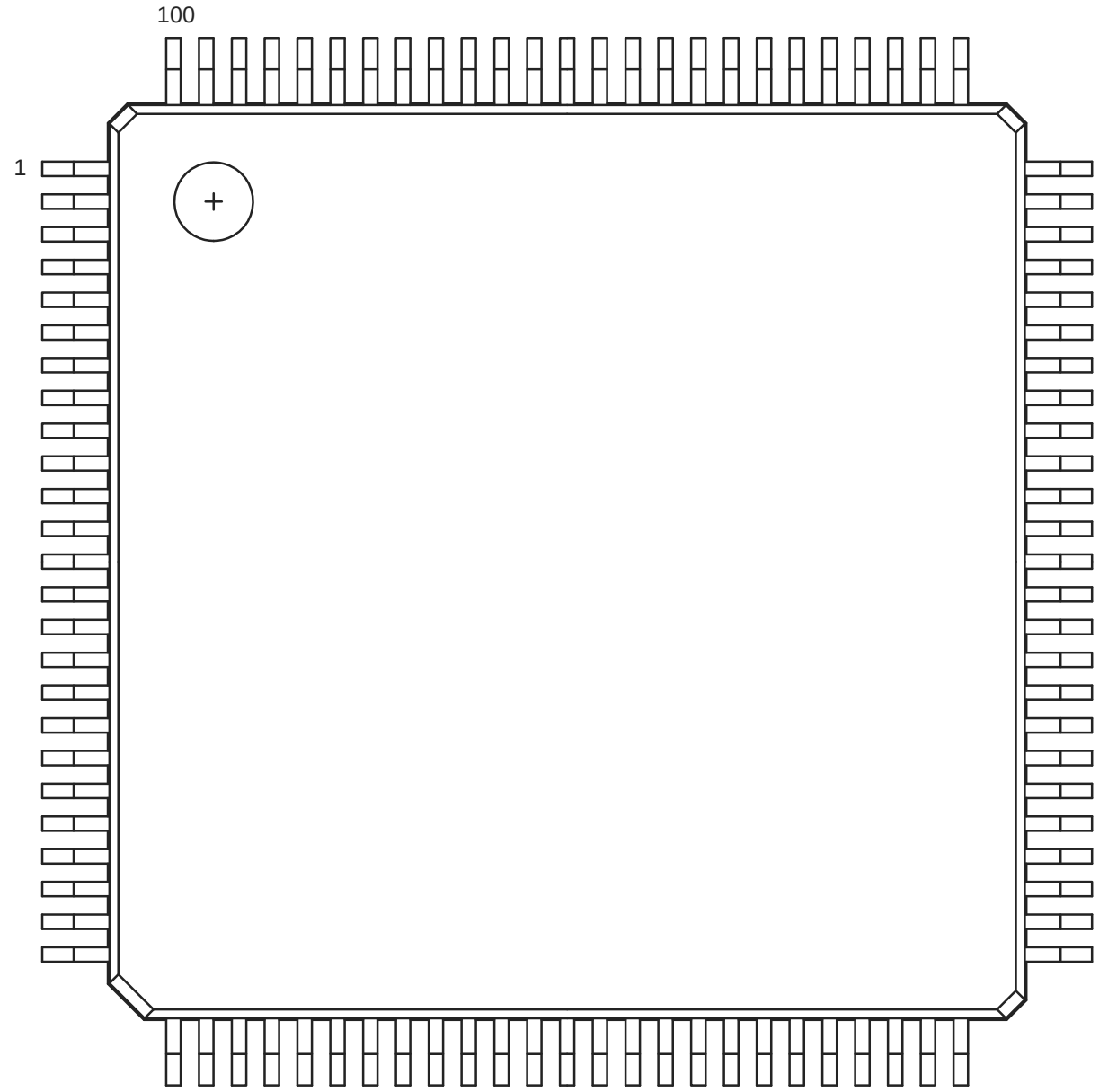
***Table 2-193* • RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

VQ100



Note: This is the top view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	**AGL400 Function**
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

FG484	
Pin Number	**AGL400 Function**
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3

FG484	
Pin Number	**AGL400 Function**
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	FF/GEB2/IO133RSB2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC

FG484	
Pin Number	**AGL1000 Function**
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

5 – Datasheet Information

List of Changes

The following tables list critical changes that were made in each revision of the IGLOO datasheet.

Revision	Changes	Page
Revision 27 (May 2016)	Added the deleted package FG144 from AGL125 device in "IGLOO Devices" (SAR 79355).	1-I
Revision 26 (March 2016)	Updated "IGLOO Ordering Information" and "Temperature Grade Offerings" notes by: • Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352). • Replacing Industrial (–40°C to +85°C Ambient Temperature) with Industrial (–40°C to +100°C Junction Temperature) (SAR 48352).	1-III and 1-IV
	Ambient temperature row removed in Table 2-2 (SAR 48352).	2-2
	Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087).	2-2
	Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087)	2-2
	Added 2 mA drive strengths in tables same as 4 mA (SAR 57179).	NA
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777).	NA
Revision 25 (June2015)	Removed package FG144 from AGL060 device in the following tables: "IGLOO Devices", "I/Os Per Package1" and "Temperature Grade Offerings" (SAR 68517)	I, II, and IV
	Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517)	-
Revision 24 (March 2014)	Note added for the discontinuance of QN132 package to the following tables: "IGLOO Devices", "I/Os Per Package1", "IGLOO FPGAs Package Sizes Dimensions", and"Temperature Grade Offerings" and "QN132" section (SAR 55117, PDN 1306).	I, II, IV, and 4-28
	Removed packages CS81 and QN132 from AGL250 device in the following tables: "IGLOO Devices", "I/Os Per Package1", and "Temperature Grade Offerings" (SAR 49472).	I, II, and IV

Revision / Version	Changes	Page
Advance v0.4 (September 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.3 (August 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2