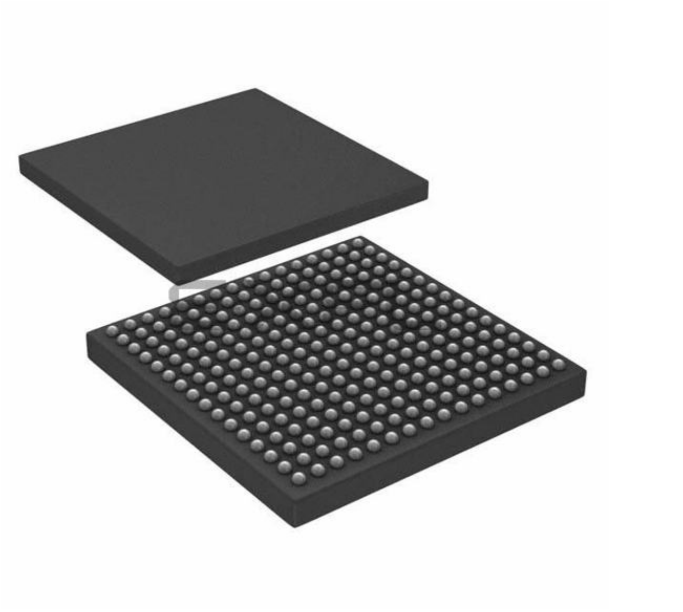

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 9216 |
| Total RAM Bits | 55296 |
| Number of I/O | 178 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agl400v5-fgg256i |

***Table 2-22 •*** **Different Components Contributing to the Static Power Consumption in IGLOO Device For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

| Parameter | Definition | Device Specific Static Power (mW) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | **AGL1000** | **AGL600** | **AGL400** | **AGL250** | **AGL125** | **AGL060** | **AGL030** | **AGL015** |
| PDC1 | Array static power in Active mode | See Table 2-12 on page 2-9. | | | | | | | |
| PDC2 | Array static power in Static (Idle) mode | See Table 2-11 on page 2-8. | | | | | | | |
| PDC3 | Array static power in Flash*Freeze mode | See Table 2-9 on page 2-7. | | | | | | | |
| PDC4 | Static PLL contribution | 0.90 | | | | | | | |
| PDC5 | Bank quiescent power (VCCI-Dependent) | See Table 2-12 on page 2-9. | | | | | | | |
| PDC6 | I/O input pin static power (standard-dependent) | See Table 2-13 on page 2-10 through Table 2-15 on page 2-11. | | | | | | | |
| PDC7 | I/O output pin static power (standard-dependent) | See Table 2-16 on page 2-11 through Table 2-18 on page 2-12. | | | | | | | |

*Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.*

# Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microsemi Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24 on page 2-19. The calculation should be repeated for each clock domain defined in the design.

## Methodology

### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

### Total Static Power Consumption—$P_{STAT}$

$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$N_{BANKS}$ is the number of I/O banks powered in the design.

### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$, $P_{AC2}$, $P_{AC3}$, and $P_{AC4}$ are device-dependent.

### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

### Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

### *Routing Net Contribution—$P_{NET}$*

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

### *I/O Input Buffer Contribution—$P_{INPUTS}$*

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

### *I/O Output Buffer Contribution—$P_{OUTPUTS}$*

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

### *RAM Contribution—$P_{MEMORY}$*

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

$\beta_3$ is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

### *PLL Contribution—$P_{PLL}$*

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

$F_{CLKOUT}$ is the output clock frequency.†

† *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

**Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.09 | 0.18 | 0.85 | 0.66 | 2.14 | 1.68 | 2.67 | 3.05 | 5.73 | 5.27 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 | High | 5 | – | 0.97 | 2.93 | 0.18 | 1.19 | 0.66 | 2.95 | 2.27 | 3.81 | 4.30 | 6.54 | 5.87 | ns |
| 2.5 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.09 | 0.18 | 1.08 | 0.66 | 2.14 | 1.83 | 2.73 | 2.93 | 5.73 | 5.43 | ns |
| 1.8 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.24 | 0.18 | 1.01 | 0.66 | 2.29 | 2.00 | 3.02 | 3.40 | 5.88 | 5.60 | ns |
| 1.5 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.50 | 0.18 | 1.17 | 0.66 | 2.56 | 2.27 | 3.21 | 3.48 | 6.15 | 5.86 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 [2] | 0.97 | 2.32 | 0.18 | 0.74 | 0.66 | 2.37 | 1.78 | 2.67 | 3.05 | 5.96 | 5.38 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 [2] | 0.97 | 2.32 | 0.19 | 0.70 | 0.66 | 2.37 | 1.78 | 2.67 | 3.05 | 5.96 | 5.38 | ns |
| LVDS | 24 mA | – | High | – | – | 0.97 | 1.74 | 0.19 | 1.35 | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | – | High | – | – | 0.97 | 1.68 | 0.19 | 1.16 | – | – | – | – | – | – | – | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

**Table 2-65 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard I/O Banks**

| 3.3 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

**Table 2-66 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

***Applies to 1.2 V Core Voltage***

***Table 2-89 •*** **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 5.59 | 0.26 | 1.20 | 1.10 | 5.68 | 5.14 | 2.82 | 2.80 | 11.47 | 10.93 | ns |
| 4 mA | Std. | 1.55 | 5.59 | 0.26 | 1.20 | 1.10 | 5.68 | 5.14 | 2.82 | 2.80 | 11.47 | 10.93 | ns |
| 6 mA | Std. | 1.55 | 4.76 | 0.26 | 1.20 | 1.10 | 4.84 | 4.47 | 3.10 | 3.33 | 10.62 | 10.26 | ns |
| 8 mA | Std. | 1.55 | 4.76 | 0.26 | 1.20 | 1.10 | 4.84 | 4.47 | 3.10 | 3.33 | 10.62 | 10.26 | ns |
| 12 mA | Std. | 1.55 | 4.17 | 0.26 | 1.20 | 1.10 | 4.23 | 3.99 | 3.30 | 3.67 | 10.02 | 9.77 | ns |
| 16 mA | Std. | 1.55 | 3.98 | 0.26 | 1.20 | 1.10 | 4.04 | 3.88 | 3.34 | 3.76 | 9.83 | 9.66 | ns |
| 24 mA | Std. | 1.55 | 3.90 | 0.26 | 1.20 | 1.10 | 3.96 | 3.90 | 3.40 | 4.09 | 9.75 | 9.68 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-90 •*** **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.33 | 0.26 | 1.20 | 1.10 | 3.38 | 3.09 | 2.82 | 2.91 | 9.17 | 8.88 | ns |
| 4 mA | Std. | 1.55 | 3.33 | 0.26 | 1.20 | 1.10 | 3.38 | 3.09 | 2.82 | 2.91 | 9.17 | 8.88 | ns |
| 6 mA | Std. | 1.55 | 2.89 | 0.26 | 1.20 | 1.10 | 2.93 | 2.56 | 3.10 | 3.45 | 8.72 | 8.34 | ns |
| 8 mA | Std. | 1.55 | 2.89 | 0.26 | 1.20 | 1.10 | 2.93 | 2.56 | 3.10 | 3.45 | 8.72 | 8.34 | ns |
| 12 mA | Std. | 1.55 | 2.64 | 0.26 | 1.20 | 1.10 | 2.67 | 2.29 | 3.30 | 3.79 | 8.46 | 8.08 | ns |
| 16 mA | Std. | 1.55 | 2.59 | 0.26 | 1.20 | 1.10 | 2.63 | 2.24 | 3.34 | 3.88 | 8.41 | 8.03 | ns |
| 24 mA | Std. | 1.55 | 2.60 | 0.26 | 1.20 | 1.10 | 2.64 | 2.18 | 3.40 | 4.22 | 8.42 | 7.97 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-91 •*** **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 5.02 | 0.26 | 1.19 | 1.10 | 5.11 | 4.60 | 2.50 | 2.62 | 10.89 | 10.38 | ns |
| 4 mA | Std. | 1.55 | 5.02 | 0.26 | 1.19 | 1.10 | 5.11 | 4.60 | 2.50 | 2.62 | 10.89 | 10.38 | ns |
| 6 mA | Std. | 1.55 | 4.21 | 0.26 | 1.19 | 1.10 | 4.27 | 4.00 | 2.76 | 3.10 | 10.06 | 9.79 | ns |
| 8 mA | Std. | 1.55 | 4.21 | 0.26 | 1.19 | 1.10 | 4.27 | 4.00 | 2.76 | 3.10 | 10.06 | 9.79 | ns |
| 12 mA | Std. | 1.55 | 3.66 | 0.26 | 1.19 | 1.10 | 3.71 | 3.55 | 2.94 | 3.41 | 9.50 | 9.34 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-107*** **• 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 6.32 | 0.26 | 1.11 | 1.10 | 6.43 | 5.81 | 2.47 | 2.16 | 12.22 | 11.60 | ns |
| 4 mA | Std. | 1.55 | 5.27 | 0.26 | 1.11 | 1.10 | 5.35 | 5.01 | 2.78 | 2.92 | 11.14 | 10.79 | ns |
| 6 mA | Std. | 1.55 | 4.56 | 0.26 | 1.11 | 1.10 | 4.64 | 4.44 | 3.00 | 3.30 | 10.42 | 10.22 | ns |
| 8 mA | Std. | 1.55 | 4.56 | 0.26 | 1.11 | 1.10 | 4.64 | 4.44 | 3.00 | 3.30 | 10.42 | 10.22 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-108*** **• 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.22 | 0.26 | 1.11 | 1.10 | 3.26 | 3.18 | 2.47 | 2.20 | 9.05 | 8.97 | ns |
| 4 mA | Std. | 1.55 | 2.72 | 0.26 | 1.11 | 1.10 | 2.75 | 2.50 | 2.78 | 3.01 | 8.54 | 8.29 | ns |
| 6 mA | Std. | 1.55 | 2.43 | 0.26 | 1.11 | 1.10 | 2.47 | 2.16 | 2.99 | 3.39 | 8.25 | 7.94 | ns |
| 8 mA | Std. | 1.55 | 2.43 | 0.26 | 1.11 | 1.10 | 2.47 | 2.16 | 2.99 | 3.39 | 8.25 | 7.94 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-109*** **• 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 6.13 | 0.26 | 1.08 | 1.10 | 6.24 | 5.79 | 2.08 | 1.78 | ns |
| 4 mA | Std. | 1.55 | 5.17 | 0.26 | 1.08 | 1.10 | 5.26 | 4.98 | 2.38 | 2.54 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-110*** **• 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 3.06 | 0.26 | 1.08 | 1.10 | 3.10 | 3.01 | 2.08 | 1.83 | 3.06 | ns |
| 4 mA | Std. | 2.60 | 0.26 | 1.08 | 1.10 | 2.64 | 2.33 | 2.38 | 2.62 | 2.60 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Input Register

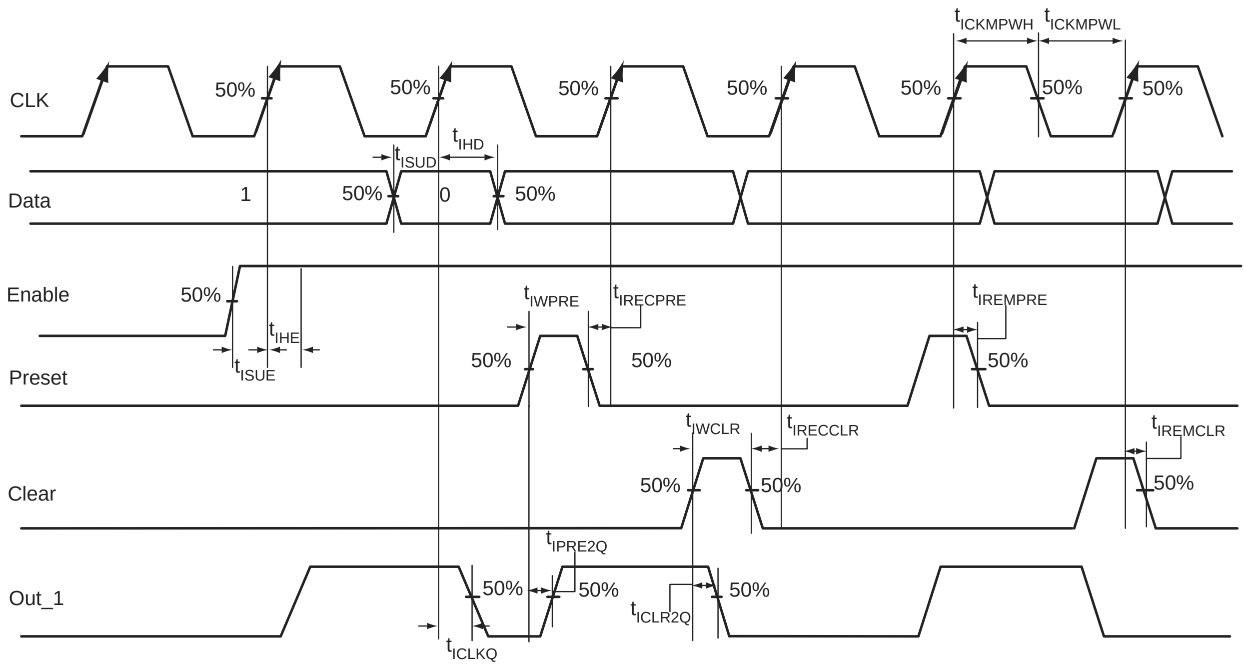


***Figure 2-18 •*** **Input Register Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-157 •*** **Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.42 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.47 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.67 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-158 • Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.68 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.97 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 1.02 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Output Register

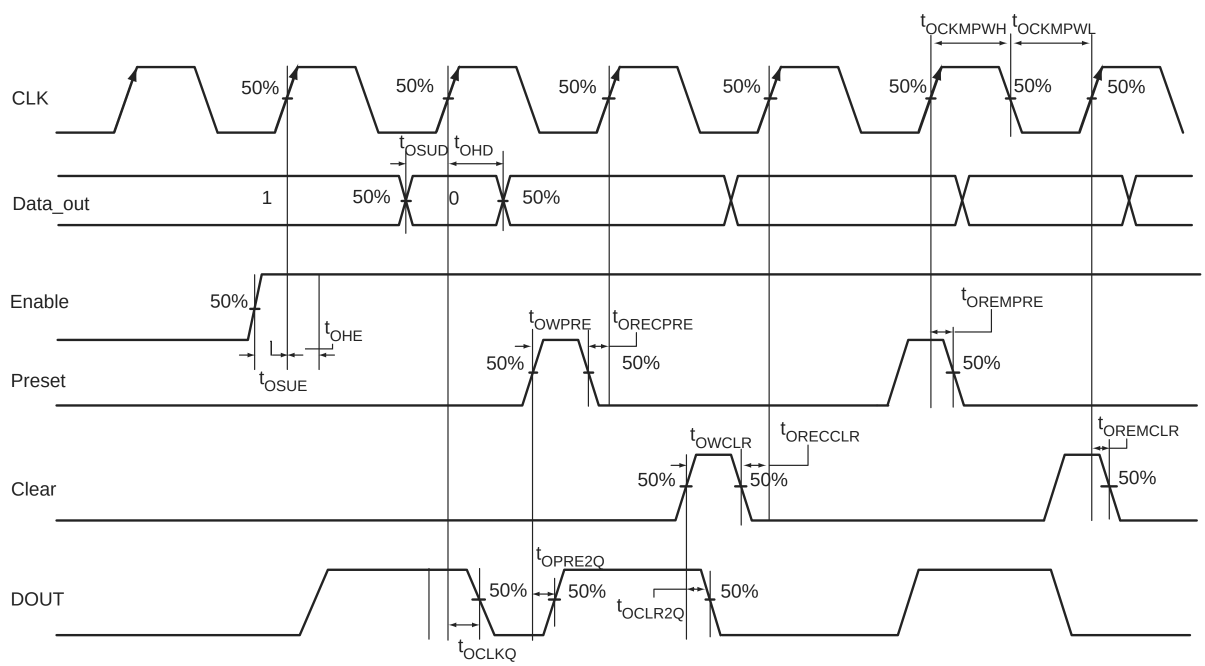


**Figure 2-19 • Output Register Timing Diagram**

### *1.2 V DC Core Voltage*

***Table 2-168 •* Output DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 1.60 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 1.09 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 1.16 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 1.99 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.24 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.19 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.31 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.28 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

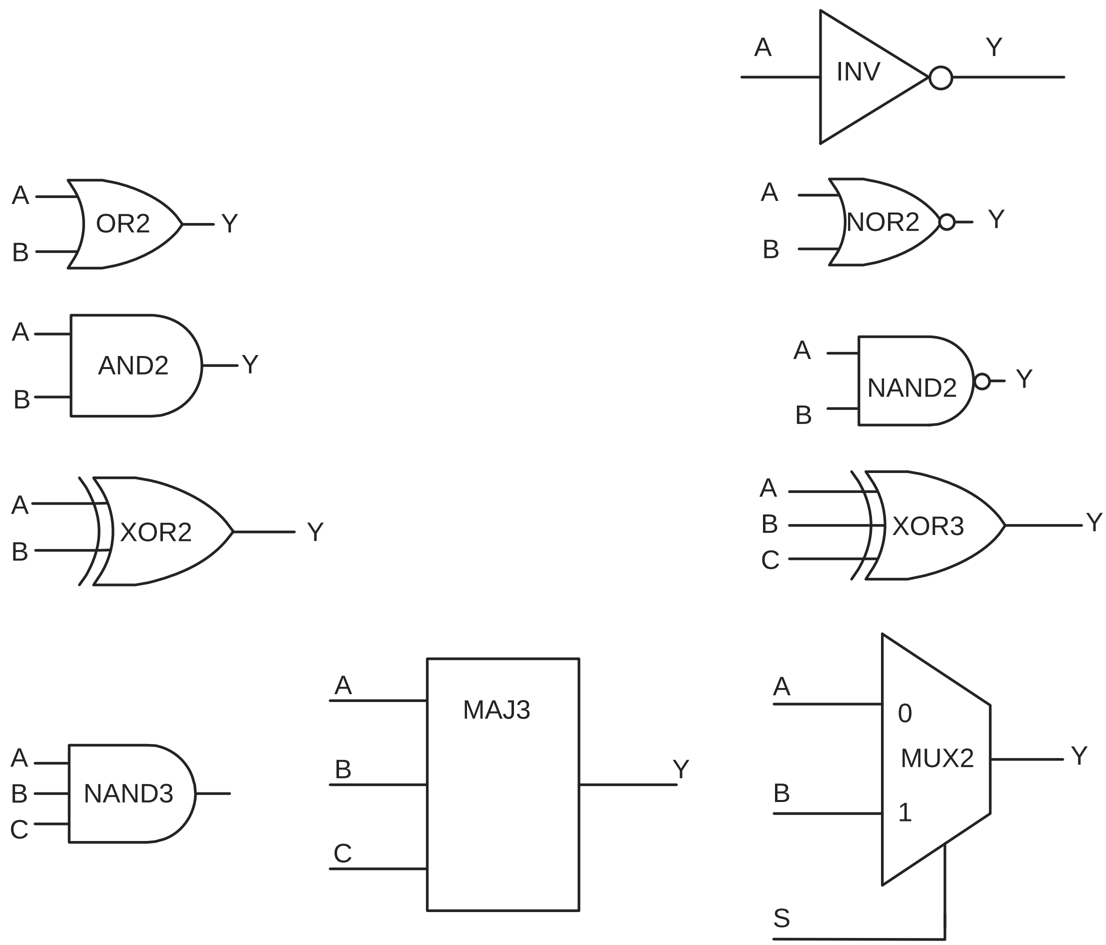


***Figure 2-25 •*** **Sample of Combinatorial Cells**

## VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

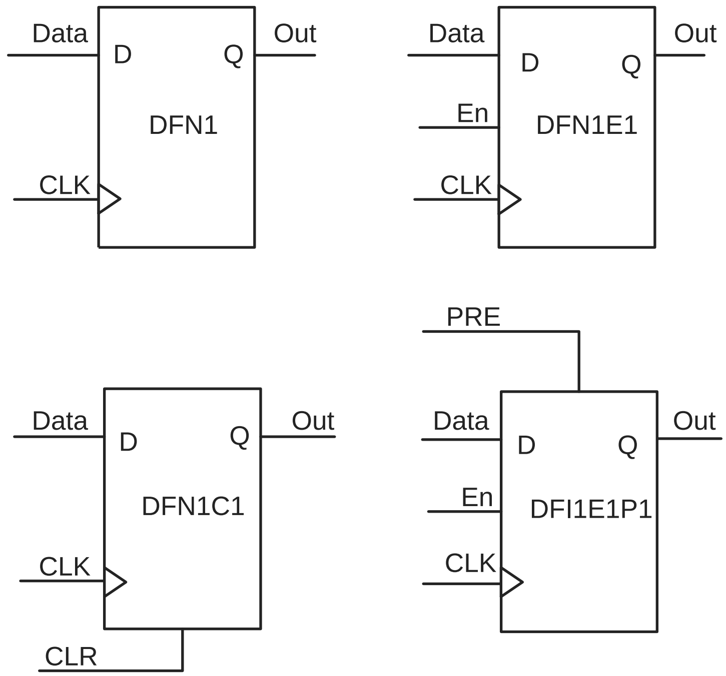


***Figure 2-27 •*** **Sample of Sequential Cells**

***Table 2-185 •*** **AGL250 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.11 | 2.57 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.19 | 2.81 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-186 •*** **AGL400 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.18 | 2.64 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.27 | 2.89 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.62 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-196* • FIFO**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 4.13 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.31 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.47 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 1.56 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.49 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 6.80 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 3.62 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 7.23 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 6.85 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 26.61 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 7.12 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 26.33 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 4.09 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 4.09 | ns |
| $t_{REMRSTB}$ | RESET Removal | 1.23 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 6.58 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 1.18 | ns |
| $t_{CYC}$ | Clock Cycle Time | 10.90 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 92 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

| CS121 | |
|---|---|
| **Pin Number** | **AGL060 Function** |
| K10 | VPUMP |
| K11 | GDB1/IO47RSB0 |
| L1 | VMV1 |
| L2 | GNDQ |
| L3 | IO65RSB1 |
| L4 | IO63RSB1 |
| L5 | IO61RSB1 |
| L6 | IO58RSB1 |
| L7 | IO57RSB1 |
| L8 | IO55RSB1 |
| L9 | GNDQ |
| L10 | GDA0/IO50RSB0 |
| L11 | VMV1 |

| FG144 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| K1 | GEB0/IO136NDB3 |
| K2 | GEA1/IO135PDB3 |
| K3 | GEA0/IO135NDB3 |
| K4 | GEA2/IO134RSB2 |
| K5 | IO127RSB2 |
| K6 | IO121RSB2 |
| K7 | GND |
| K8 | IO104RSB2 |
| K9 | GDC2/IO82RSB2 |
| K10 | GND |
| K11 | GDA0/IO79VDB1 |
| K12 | GDB0/IO78VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | FF/GEB2/IO133RSB2 |
| L4 | IO128RSB2 |
| L5 | VCCIB2 |
| L6 | IO119RSB2 |
| L7 | IO114RSB2 |
| L8 | IO110RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO132RSB2 |
| M3 | IO129RSB2 |
| M4 | IO126RSB2 |
| M5 | IO124RSB2 |
| M6 | IO122RSB2 |
| M7 | IO117RSB2 |
| M8 | IO115RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG484 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| E13 | IO38RSB0 |
| E14 | IO42RSB0 |
| E15 | GBC1/IO55RSB0 |
| E16 | GBB0/IO56RSB0 |
| E17 | IO44RSB0 |
| E18 | GBA2/IO60PDB1 |
| E19 | IO60NDB1 |
| E20 | GND |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO154VDB3 |
| F5 | IO155VDB3 |
| F6 | IO11RSB0 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO45RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO48RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | NC |
| G2 | NC |
| G3 | NC |
| G4 | IO151VDB3 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| E13 | IO38RSB0 |
| E14 | IO42RSB0 |
| E15 | GBC1/IO55RSB0 |
| E16 | GBB0/IO56RSB0 |
| E17 | IO52RSB0 |
| E18 | GBA2/IO60PDB1 |
| E19 | IO60NDB1 |
| E20 | GND |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO173NDB3 |
| F5 | IO174NDB3 |
| F6 | VMV3 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO44RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO51RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | IO170NDB3 |
| G2 | IO170PDB3 |
| G3 | NC |
| G4 | IO171NDB3 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| U1 | IO149PDB3 |
| U2 | IO149NDB3 |
| U3 | NC |
| U4 | GEB1/IO145PDB3 |
| U5 | GEB0/IO145NDB3 |
| U6 | VMV2 |
| U7 | IO138RSB2 |
| U8 | IO136RSB2 |
| U9 | IO131RSB2 |
| U10 | IO124RSB2 |
| U11 | IO119RSB2 |
| U12 | IO107RSB2 |
| U13 | IO104RSB2 |
| U14 | IO97RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO88NDB1 |
| U20 | NC |
| U21 | IO83NDB1 |
| U22 | NC |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO144PDB3 |
| V5 | GEA0/IO144NDB3 |
| V6 | IO139RSB2 |
| V7 | GEC2/IO141RSB2 |
| V8 | IO132RSB2 |
| V9 | IO127RSB2 |
| V10 | IO121RSB2 |
| V11 | IO114RSB2 |
| V12 | IO109RSB2 |
| V13 | IO105RSB2 |
| V14 | IO98RSB2 |

| Revision | Changes | Page |
|---|---|---|
| Revision 19 (continued) | The following sentence was removed from the "Advanced Architecture" section:<br>"In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756). | 1-3 |
| | The "Specifying I/O States During Programming" section is new (SAR 21281). | 1-8 |
| | Values for VCCPLL at 1.2 V –1.5 V DC core supply voltage were revised in Table 2-2 • Recommended Operating Conditions 1 (SAR 22356).<br>The value for VPUMP operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 25220).<br>The value for VCCPLL 1.5 V DC core supply voltage was changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 26551).<br>The notes in the table were renumbered in order of their appearance in the table (SAR 21869). | 2-2 |
| | The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2 • Recommended Operating Conditions 1. The resulting maximum power allowed is thus 1.28 W. Formerly it was 1.71 W (SAR 26259). | 2-6 |
| | Values for CS196, CS281, and QN132 packages were added to Table 2-5 • Package Thermal Resistivities (SARs 26228, 32301). | 2-6 |
| | Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041). | 2-7 |
| | The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD (SAR 24112). Table 2-8 • Power Supply State per Mode is new. | 2-7 |
| | The formulas in the table notes for Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 21348). | 2-37 |
| | The row for 110°C was removed from Table 2-45 • Duration of Short Circuit Event before Failure. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was revised to change 110° to 100°C. (SAR 26259). | 2-40 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700). | 2-28, 2-47, 2-77 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-56 |
| | The values for $F_{DDRIMAX}$ and $F_{DDOMAX}$ were updated in the tables in the "Input DDR Module" section and "Output DDR Module" section (SAR 23919). | 2-94, 2-97 |
| | The following notes were removed from Table 2-147 • Minimum and Maximum DC Input and Output Levels (SAR 29428):<br>±5%<br>Differential input voltage = ±350 mV | 2-81 |
| | Table 2-189 • IGLOO CCC/PLL Specification and Table 2-190 • IGLOO CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705). | 2-115 |