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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	177
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl600v2-fgg256

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note: IDD = N_{BANKS} × ICCI. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode**

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	µA

Table 2-12 • **Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode[1]**

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
ICCA Current[2]										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	µA
	1.5 V	14	16	20	28	44	66	82	137	µA
ICCI or IJTAG Current[3]										
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Notes:

1. *IDD = N_{BANKS} × ICCI + ICCA. JTAG counts as one bank when powered.*
2. *Includes VCC, VPUMP, and VCCPLL currents.*
3. *Values do not include I/O static contribution (PDC6 and PDC7).*

Table 2-39 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS[4]	2 mA	158	164
1.2 V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{OHspec}$
4. *Applicable to IGLOO V2 Devices operating at VCCI ≥ VCC*

Table 2-40 • I/O Output Buffer Maximum Resistances[1]
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	158	164
1.2 V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{OHspec}$

Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V Wide Range I/Os	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-51 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-52 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-53 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-54 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-55 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-56 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-62 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-111 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-112 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

1.2 V DC Core Voltage

Table 2-145 • 3.3 V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-146 • 3.3 V PCI/PCI-X
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOO also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

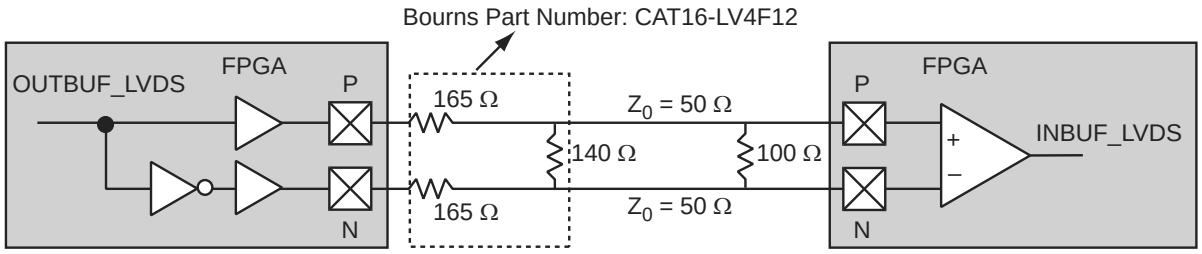

Figure 2-13 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-147 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL[1]	Output Lower Current	0.65	0.91	1.16	mA
IOH[1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH[2]	Input High Leakage Current			10	µA
IIL[2]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF[4]	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH is defined by VODIFF/(resistor network)*
2. *Currents are measured at 85°C junction temperature.*

Table 2-148 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-149 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-150 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.19	0.25	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-169 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y =!A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y =!(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-170 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.34	ns
AND2	Y = A · B	t_{PD}	1.43	ns
NAND2	Y = !(A · B)	t_{PD}	1.59	ns
OR2	Y = A + B	t_{PD}	2.30	ns
NOR2	Y = !(A + B)	t_{PD}	2.07	ns
XOR2	Y = A ⊕ B	t_{PD}	2.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.46	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.12	ns
MUX2	Y = A !S + B S	t_{PD}	2.83	ns
AND3	Y = A · B · C	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Resource Characteristics

AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 2-29 is an example of a global tree used for clock routing. The global tree presented in Figure 2-29 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

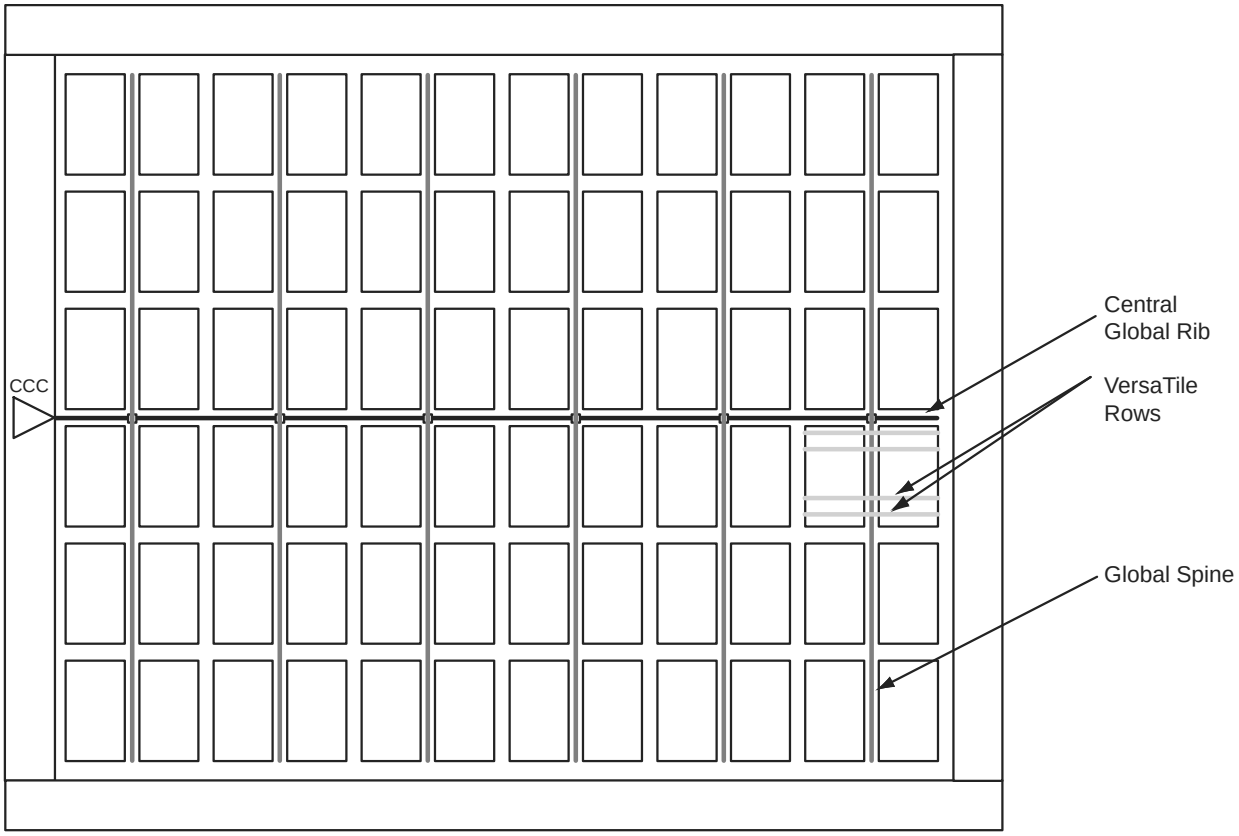

Figure 2-29 • **Example of Global Tree Use in an AGL250 Device for Clock Routing**

Table 2-177 • **AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-178 • **AGL400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min. [1]	Max. [2]	
t_{RCKL}	Input Low Delay for Global Clock	1.45	1.79	ns
t_{RCKH}	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-185 • **AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-186 • **AGL400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.18	2.64	ns
t_{RCKH}	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

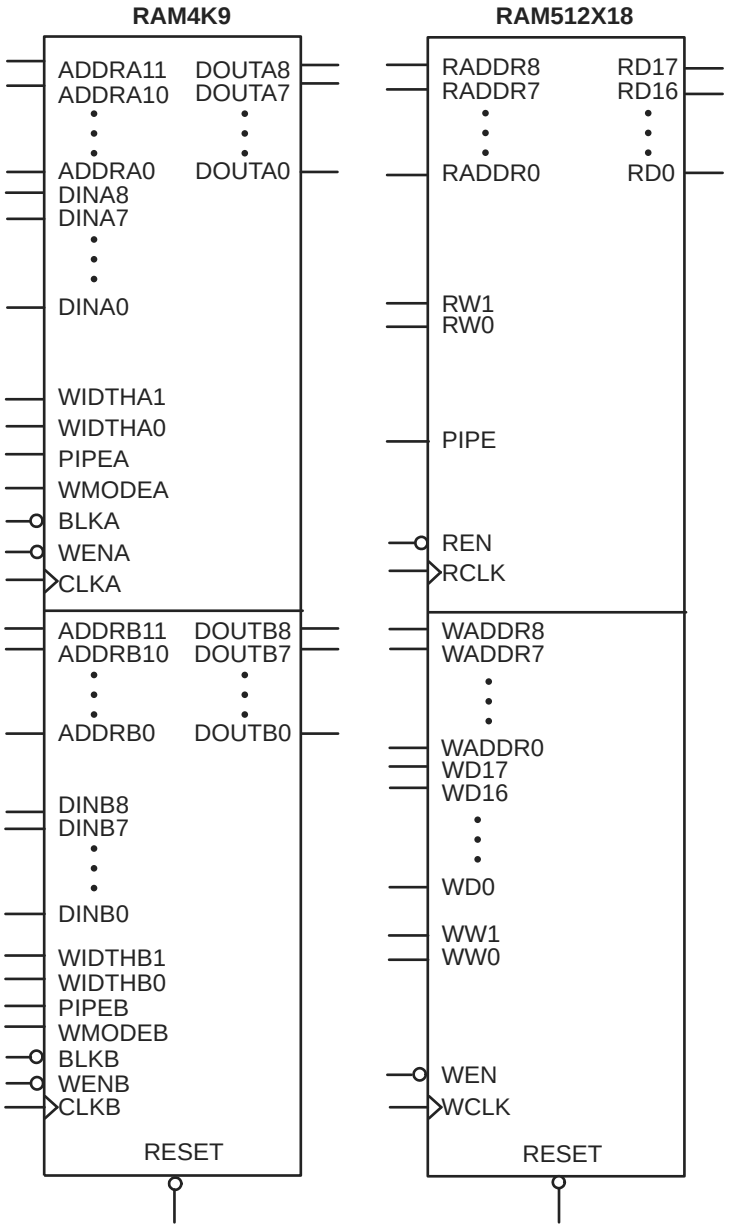

Figure 2-31 • **RAM Models**

Table 2-194 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN, WEN setup time	1.36	ns
t_{ENH}	REN, WEN hold time	0.15	ns
t_{DS}	Input data (WD) setup time	1.33	ns
t_{DH}	Input data (WD) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	7.88	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	3.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.87	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.04	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	3.86	ns
	RESET Low to data out Low on RD (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

CS281	
Pin Number	**AGL600 Function**
R15	IO94RSB2
R16	GDA1/IO88PPB1
R18	GDB0/IO87NPB1
R19	GDC0/IO86NPB1
T1	IO148PPB3
T2	GEC0/IO146NPB3
T4	GEB0/IO145NPB3
T5	IO132RSB2
T6	IO136RSB2
T7	IO130RSB2
T8	IO126RSB2
T9	IO120RSB2
T10	GND
T11	IO113RSB2
T12	IO104RSB2
T13	IO101RSB2
T14	IO98RSB2
T15	GDC2/IO91RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO87PPB1
U1	IO147PDB3
U2	GEA1/IO144PPB3
U6	IO131RSB2
U14	IO99RSB2
U18	TRST
U19	GDA0/IO88NPB1
V1	IO147NDB3
V2	VCCIB3
V3	GEC2/IO141RSB2
V4	IO140RSB2
V5	IO135RSB2
V6	GND
V7	IO125RSB2
V8	IO122RSB2
V9	IO116RSB2

CS281	
Pin Number	**AGL600 Function**
V10	IO112RSB2
V11	IO110RSB2
V12	IO108RSB2
V13	IO102RSB2
V14	GND
V15	IO93RSB2
V16	GDA2/IO89RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO142RSB2
W3	IO139RSB2
W4	IO137RSB2
W5	IO134RSB2
W6	IO133RSB2
W7	IO128RSB2
W8	IO124RSB2
W9	IO119RSB2
W10	VCCIB2
W11	IO109RSB2
W12	IO107RSB2
W13	IO105RSB2
W14	IO100RSB2
W15	IO96RSB2
W16	IO92RSB2
W17	GDB2/IO90RSB2
W18	TCK
W19	GND

FG484	
Pin Number	**AGL600 Function**
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	**AGL1000 Function**
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1

FG484	
Pin Number	**AGL1000 Function**
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1

Revision	Changes	Page
Revision 19 (continued)	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 21281).	1-8
	Values for VCCPLL at 1.2 V –1.5 V DC core supply voltage were revised in Table 2-2 • Recommended Operating Conditions 1 (SAR 22356). The value for VPUMP operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 25220). The value for VCCPLL 1.5 V DC core supply voltage was changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 26551). The notes in the table were renumbered in order of their appearance in the table (SAR 21869).	2-2
	The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2 • Recommended Operating Conditions 1. The resulting maximum power allowed is thus 1.28 W. Formerly it was 1.71 W (SAR 26259).	2-6
	Values for CS196, CS281, and QN132 packages were added to Table 2-5 • Package Thermal Resistivities (SARs 26228, 32301).	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041).	2-7
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD (SAR 24112). Table 2-8 • Power Supply State per Mode is new.	2-7
	The formulas in the table notes for Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 21348).	2-37
	The row for 110°C was removed from Table 2-45 • Duration of Short Circuit Event before Failure. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was revised to change 110° to 100°C. (SAR 26259).	2-40
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-28, 2-47, 2-77
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-56
	The values for $F_{DDRIMAX}$ and F_{DDOMAX} were updated in the tables in the "Input DDR Module" section and "Output DDR Module" section (SAR 23919).	2-94, 2-97
	The following notes were removed from Table 2-147 • Minimum and Maximum DC Input and Output Levels (SAR 29428): ±5% Differential input voltage = ±350 mV	2-81
	Table 2-189 • IGLOO CCC/PLL Specification and Table 2-190 • IGLOO CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).	2-115