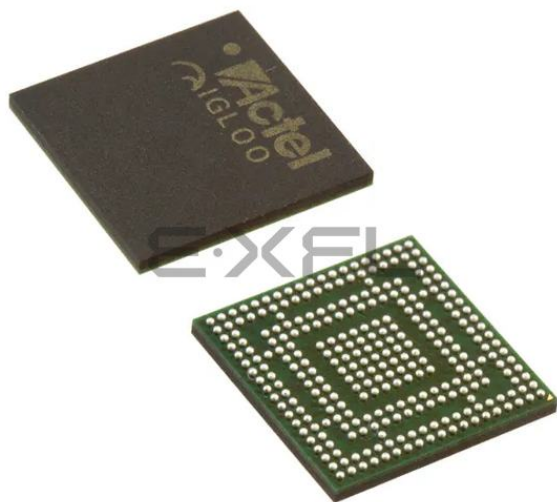




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	215
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl600v5-csg281

I/Os Per Package¹

IGLOO Devices	AGL015 ²	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250				M1AGL600		M1AGL1000	
Package	I/O Type ³											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs
QN48	–	34	–	–	–	–	–	–	–	–	–	–
QN68	49	49	–	–	–	–	–	–	–	–	–	–
UC81	–	66	–	–	–	–	–	–	–	–	–	–
CS81	–	66	–	–	–	–	–	–	–	–	–	–
CS121	–	–	96	96	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–	–	–	–	–
QN132 ⁶	–	81	80	84	–	–	–	–	–	–	–	–
CS196	–	–	–	133	143 ⁵	35 ⁵	143	35	–	–	–	–
FG144	–	–	–	97	97	24	97	25	97	25	97	25
FG256 ⁷	–	–	–	–	–	–	178	38	177	43	177	44
CS281	–	–	–	–	–	–	–	–	215	53	215	53
FG484 ⁷	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the IGLOO FPGA Fabric User Guide to ensure compliance with design and board migration requirements.
- AGL015 is not recommended for new designs.
- When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- The M1AGL250 device does not support QN132 or CS196 packages.
- Package not available.
- FG256 and FG484 are footprint-compatible packages.

Table 1 • IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23
Nominal Area (mm ²)	16	25	36	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

Note: * Package not available.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microsemi Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24 on page 2-19. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min.V	Max. V	Min. V	Max.V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS ⁴	2 mA	2 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	2 mA	High	−0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI − 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI $\geq$ VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

Table 2-33 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case
Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8	High	5	–	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
3.3 V LVCMOS Wide Range ²	100 μA	8	High	5	–	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	ns
2.5 V LVCMOS	8 mA	8	High	5	–	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
1.8 V LVCMOS	4 mA	4	High	5	–	0.97	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	ns
1.5 V LVCMOS	2 mA	2	High	5	–	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-40 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{OH_{spec}}$

Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK PULL-UP)}$ ¹ (Ω)		$R_{(WEAK PULL-DOWN)}$ ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V Wide Range I/Os	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULLDOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULLDOWN-MIN)}$

Table 2-71 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 μA	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 μA	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 μA	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-72 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 μA	4 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 μA	6 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 μA	8 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

Table 2-77 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 μA	4 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 μA	6 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns
100 μA	8 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-78 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	2 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 μA	4 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 μA	6 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
100 μA	8 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

Table 2-107 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-108 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-109 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-110 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

Table 2-127 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-128 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

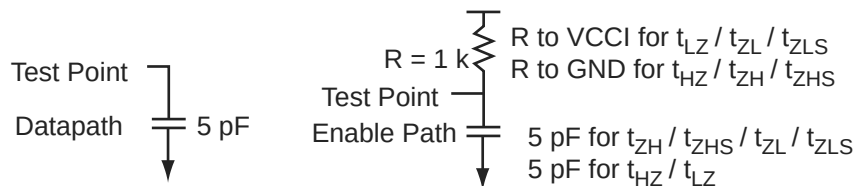
1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-129 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
1 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-11 • AC Loading****Table 2-130 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-131 • 1.2 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-132 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-133 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-134 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-189 • IGLOO CCC/PLL Specification
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		360 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{4, 5}			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁶				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.469		15.65	ns
Delay Range in Block: Fixed Delay ^{1, 2}		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data ⁷			
	SSO $\geq 4^8$	SSO $\geq 8^8$	SSO $\geq 16^8$	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. The AGL030 device does not support a PLL.
5. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
7. Measurements done with LVTTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.

Table 2-190 • IGLOO CCC/PLL Specification
For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		580 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{4,5}			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁶				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay ^{1,2}	2.3		20.86	ns
Delay Range in Block: Programmable Delay ^{2,1,2}	0.863		20.86	ns
Delay Range in Block: Fixed Delay ^{1, 2, 5}		5.7		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data ^{7,8}			
	SSO ≥ 4 ⁹	SSO ≥ 8 ⁹	SSO ≥ 16 ⁹	
0.75 MHz to 50 MHz	1.20%	2.00%	3.00%	
50 MHz to 160 MHz	5.00%	7.00%	15.00%	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.2\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
5. The AGL030 device does not support a PLL.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
7. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.
8. Measurements done with LVTTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
9. SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.
10. For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the IGLOO FPGA Fabric User Guide.

Timing Waveforms

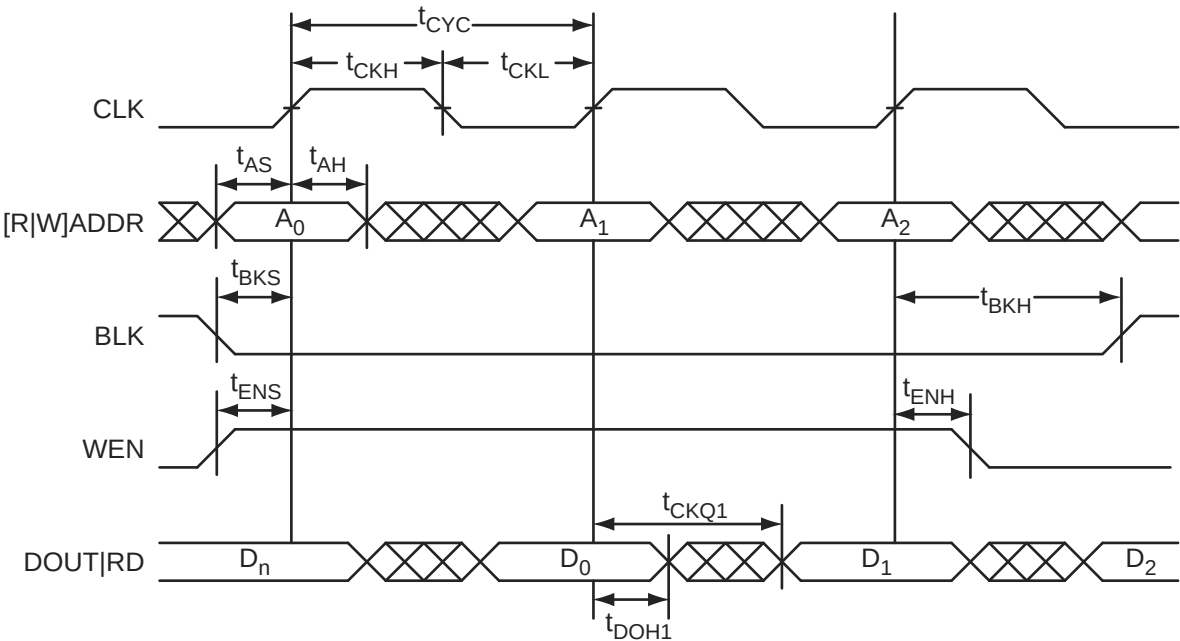


Figure 2-32 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

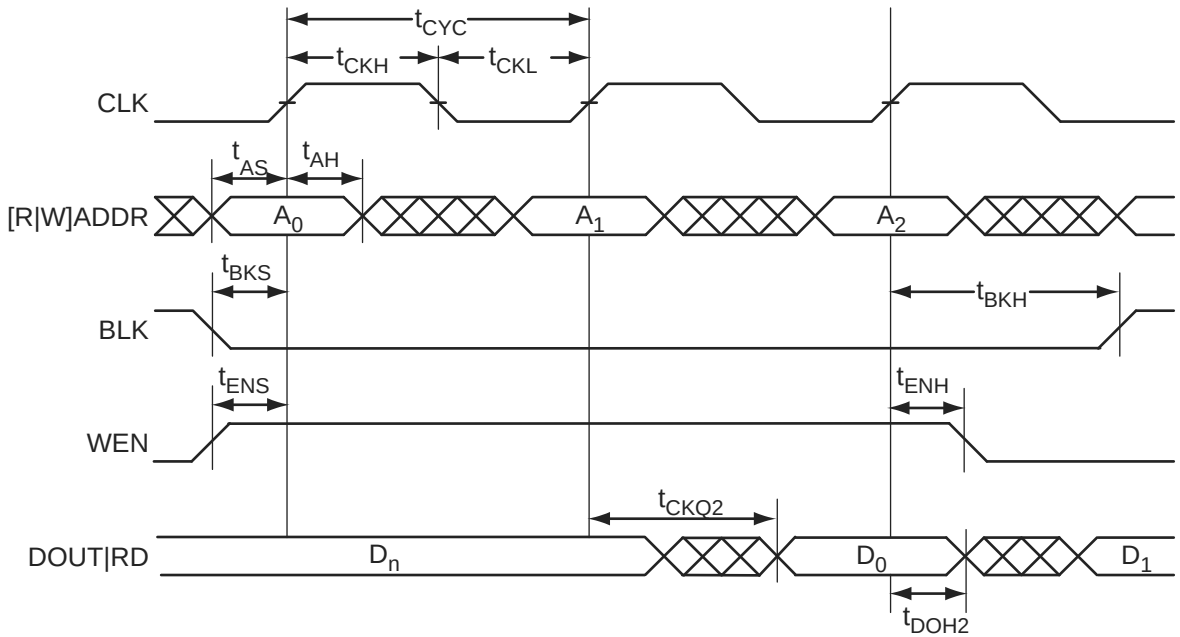


Figure 2-33 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO a devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO FPGA Fabric User Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)

IGLOO Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
CS281	W2
QN48	14
QN68	18
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

CS196	
Pin Number	AGL250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0

CS196	
Pin Number	AGL250 Function
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3

CS196	
Pin Number	AGL250 Function
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1

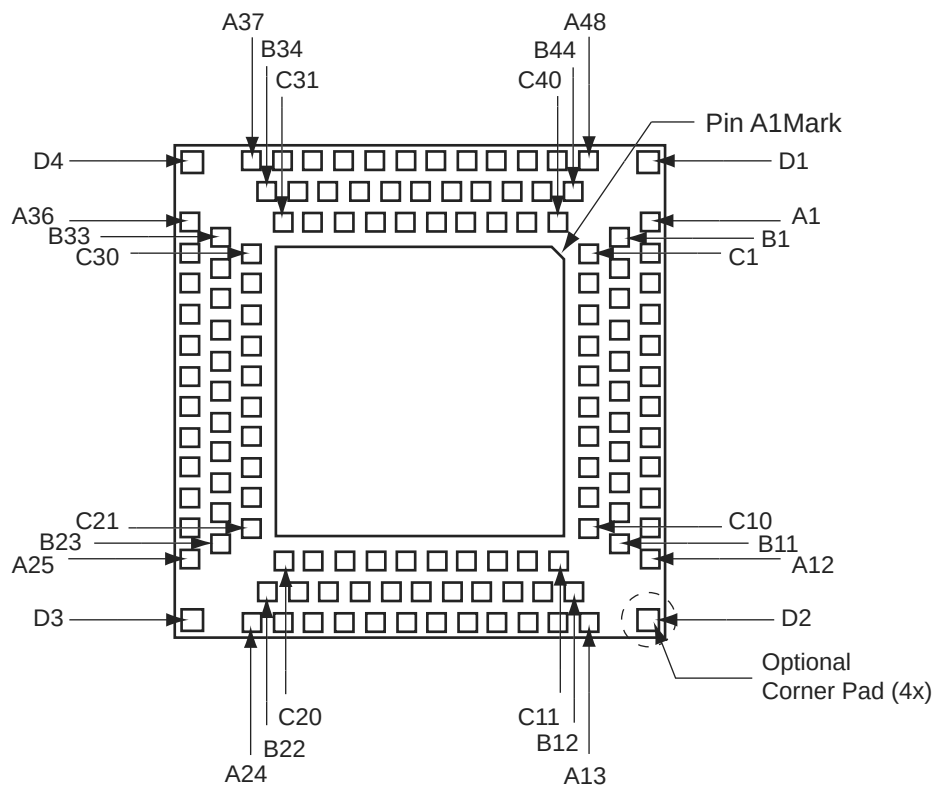
QN48	
Pin Number	AGL030 Function
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0

QN48	
Pin Number	AGL030 Function
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

QN68	
Pin Number	AGL030 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	AGL030 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Note

QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see PD3068: *Package Mechanical Drawings*.

FG256	
Pin Number	AGL1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	AGL1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	AGL1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG484	
Pin Number	AGL600 Function
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

FG484	
Pin Number	AGL600 Function
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0

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Pin Number	AGL600 Function
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC