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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	177
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl600v5-fgg256i

field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs.

† The AGL015 and AGL030 do not support PLL or SRAM.

Table 2-2 • **Recommended Operating Conditions** [1]

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature [2]		0 to +85	–40 to +100	°C
VCC[3]	1.5 V DC core supply voltage[5]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range DC core supply voltage [4,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[5]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V – 1.5 V DC core supply voltage[4,6]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [9]	1.2 V DC core supply voltage[6]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range DC supply voltage[6]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-24. VCCI should be at the same voltage within a given I/O bank.*
4. *All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
5. *For IGLOO® V5 devices*
6. *For IGLOO V2 devices only, operating at VCCI ≥ VCC.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
9. *VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information.*
10. *3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.*

Table 2-44 • **I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16
1.2 V LVCMOS	1 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26

*Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-45 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
–20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-46 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability1**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

Note: The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-62 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-107 • **1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-108 • **1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-109 • **1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-110 • **1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

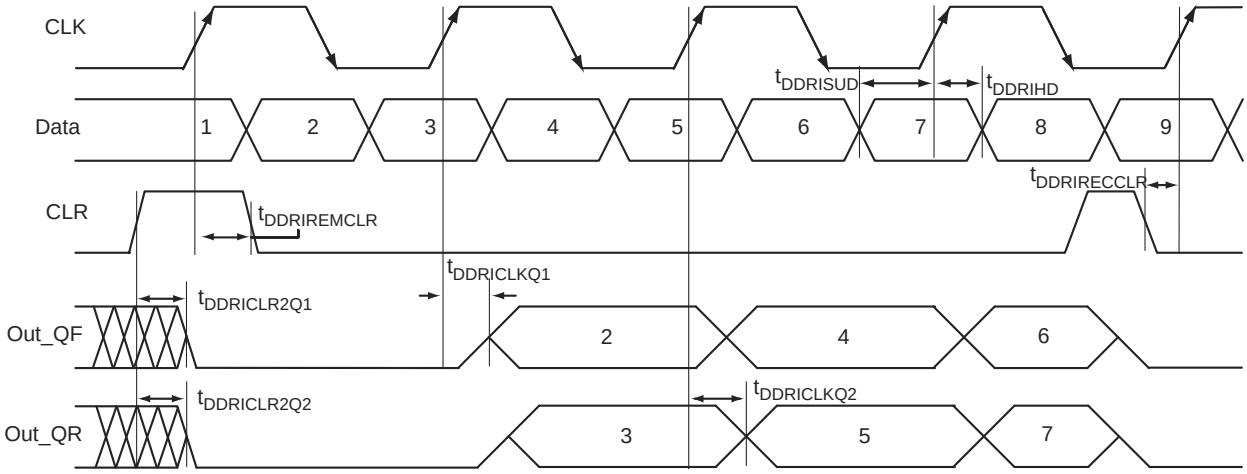


Figure 2-22 • **Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

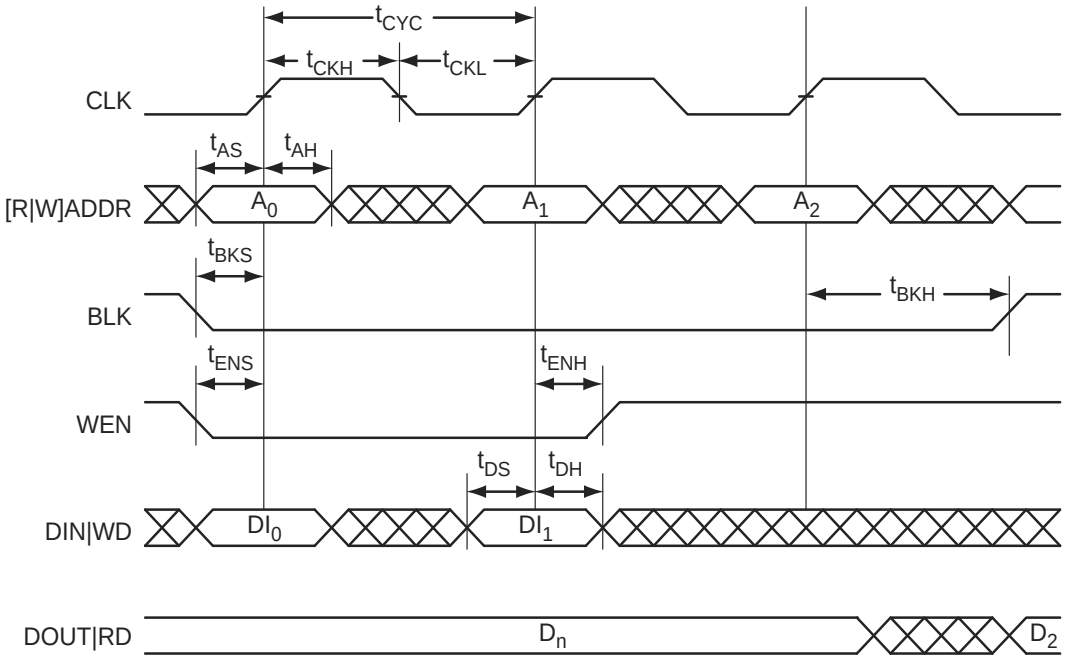


Figure 2-34 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

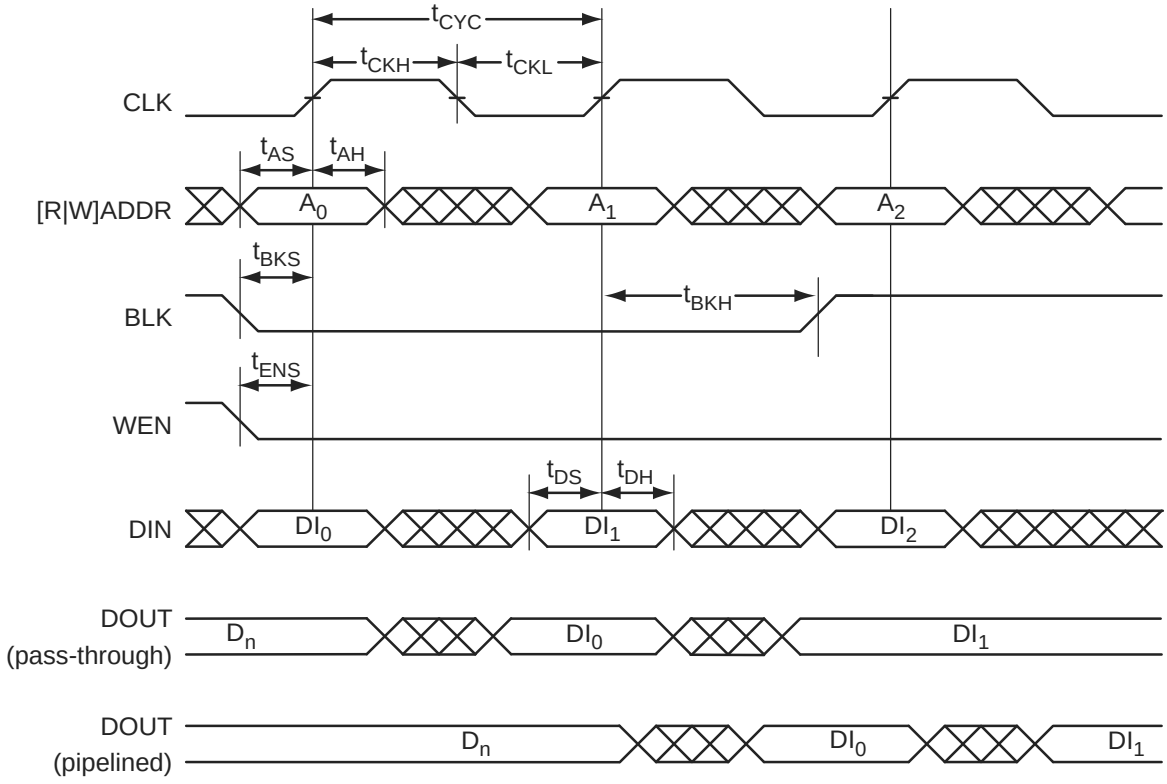


Figure 2-35 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

1.2 V DC Core Voltage

***Table 2-196* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.13	ns
t_{ENH}	REN, WEN Hold Time	0.31	ns
t_{BKS}	BLK Setup Time	0.47	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.56	ns
t_{DH}	Input Data (WD) Hold Time	0.49	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	6.80	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.62	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK High to Full Flag Valid	6.85	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	4.09	ns
	RESET Low to Data Out Low on RD (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET Removal	1.23	ns
$t_{RECRSTB}$	RESET Recovery	6.58	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

3 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices, and 1.2 V or 1.5 V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

- 1.5 V for IGLOO V5 devices
- 1.2 V or 1.5 V for IGLOO V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

- There is one VCCPLF pin on IGLOO devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.

JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

***Table 3-2* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

***Table 3-3* • TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

CS81	
Pin Number	**AGL030 Function**
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

CS81	
Pin Number	**AGL030 Function**
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	**AGL030 Function**
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	**AGL250 Function**
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO21RSB0
A6	IO27RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41PPB1
B1	GAA2/IO118UPB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO23RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO41NPB1
B9	GBB2/IO42PSB1
C1	GAB2/IO117UPB3
C2	IO118VPB3
C3	GND
C4	IO15RSB0
C5	IO25RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO43PDB1
C9	IO43NDB1
D1	GAC2/IO116USB3
D2	IO117VPB3
D3	GFA2/IO107PSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO52NPB1
D8	GCC1/IO48PDB1
D9	GCC0/IO48NDB1

CS81	
Pin Number	**AGL250 Function**
E1	GFB0/IO109NDB3
E2	GFB1/IO109PDB3
E3	GFA1/IO108PSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO50NDB1
E8	GCA1/IO50PDB1
E9	GCB2/IO52PPB1
F1	VCCPLF
F2	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO60USB1
F8	GDC1/IO58UDB1
F9	GDC0/IO58VDB1
G1	GEA0/IO98NDB3
G2	GEC1/IO100PDB3
G3	GEC0/IO100NDB3
G4	IO91RSB2
G5	IO86RSB2
G6	IO71RSB2
G7	GDB2/IO62RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO98PDB3
H2	FF/GEB2/IO96RSB2
H3	IO93RSB2
H4	IO90RSB2
H5	IO85RSB2
H6	IO77RSB2
H7	GDA2/IO61RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	**AGL250 Function**
J1	GEA2/IO97RSB2
J2	GEC2/IO95RSB2
J3	IO92RSB2
J4	IO88RSB2
J5	IO84RSB2
J6	IO74RSB2
J7	TCK
J8	TMS
J9	VPUMP

CS196	
Pin Number	**AGL250 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0

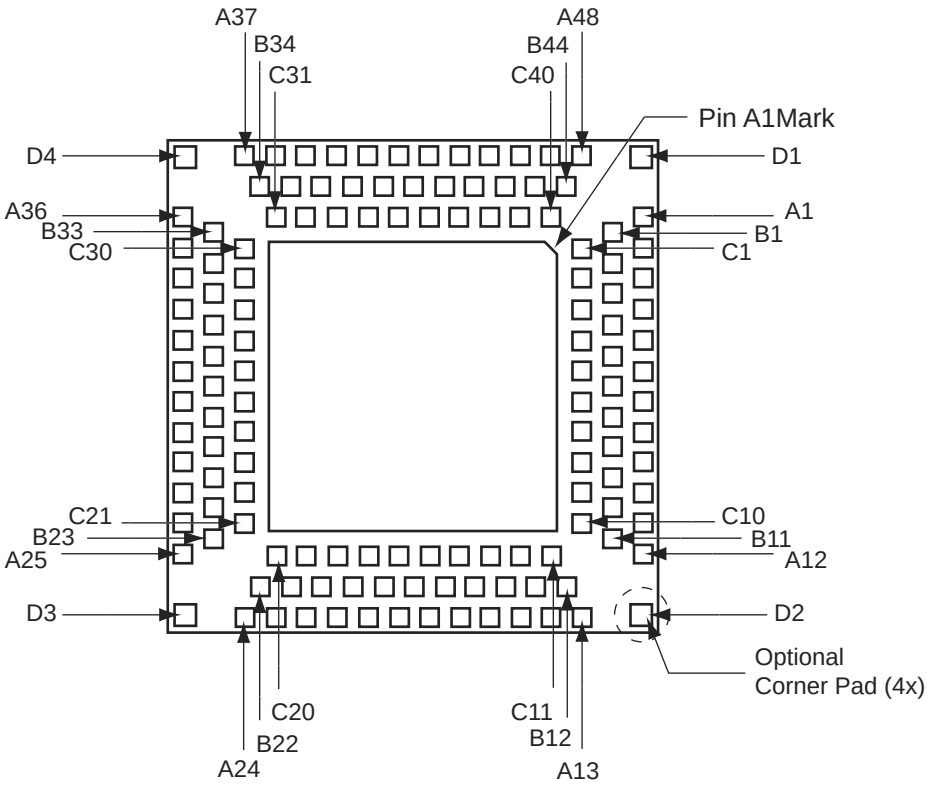
CS196	
Pin Number	**AGL250 Function**
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3

CS196	
Pin Number	**AGL250 Function**
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1

QN68	
Pin Number	**AGL030 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	**AGL030 Function**
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

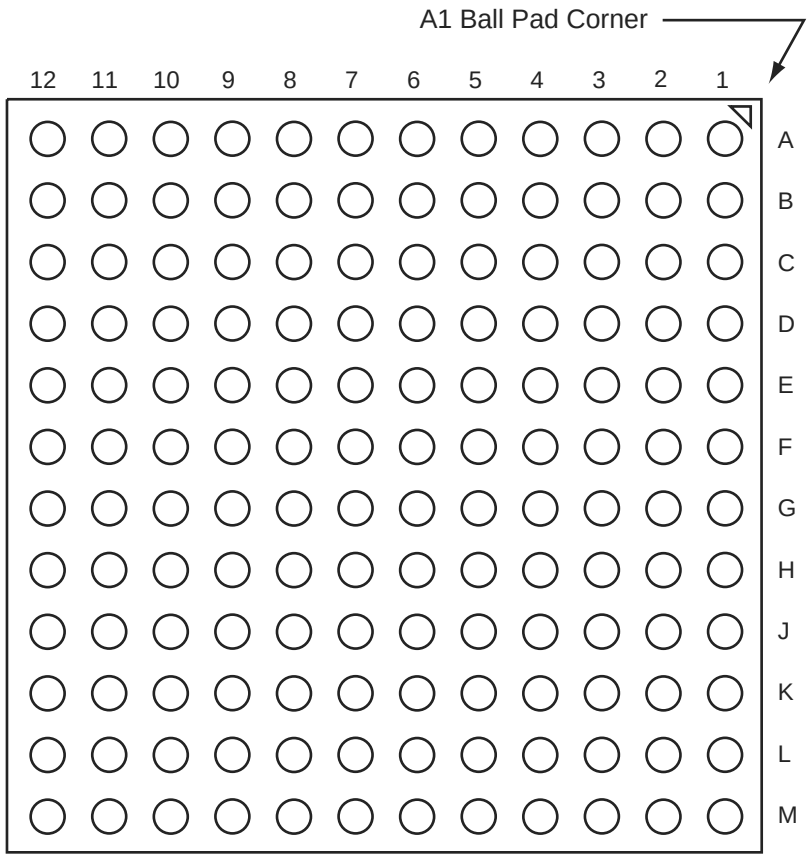
QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN132	
Pin Number	**AGL030 Function**
A1	IO80RSB1
A2	IO77RSB1
A3	NC
A4	IO76RSB1
A5	GEC0/IO73RSB1
A6	NC
A7	GEB0/IO71RSB1
A8	IO69RSB1
A9	NC
A10	VCC
A11	IO67RSB1
A12	IO64RSB1
A13	IO59RSB1
A14	IO56RSB1
A15	NC
A16	IO55RSB1
A17	IO53RSB1
A18	VCC
A19	IO50RSB1
A20	IO48RSB1
A21	IO45RSB1
A22	IO44RSB1
A23	IO43RSB1
A24	TDI
A25	TRST
A26	IO40RSB0
A27	NC
A28	IO39RSB0
A29	IO38RSB0
A30	IO36RSB0
A31	IO35RSB0
A32	GDC0/IO32RSB0
A33	NC
A34	VCC
A35	IO30RSB0
A36	IO27RSB0

QN132	
Pin Number	**AGL030 Function**
A37	IO22RSB0
A38	IO19RSB0
A39	NC
A40	IO18RSB0
A41	IO16RSB0
A42	IO14RSB0
A43	VCC
A44	IO11RSB0
A45	IO08RSB0
A46	IO06RSB0
A47	IO05RSB0
A48	IO02RSB0
B1	IO81RSB1
B2	IO78RSB1
B3	GND
B4	IO75RSB1
B5	NC
B6	GND
B7	IO70RSB1
B8	NC
B9	GND
B10	IO66RSB1
B11	IO63RSB1
B12	FF/IO60RSB1
B13	IO57RSB1
B14	GND
B15	IO54RSB1
B16	IO52RSB1
B17	GND
B18	IO49RSB1
B19	IO46RSB1
B20	GND
B21	IO42RSB1
B22	TMS
B23	TDO
B24	IO41RSB0

QN132	
Pin Number	**AGL030 Function**
B25	GND
B26	NC
B27	IO37RSB0
B28	GND
B29	GDA0/IO33RSB0
B30	NC
B31	GND
B32	IO29RSB0
B33	IO26RSB0
B34	IO23RSB0
B35	IO20RSB0
B36	GND
B37	IO17RSB0
B38	IO15RSB0
B39	GND
B40	IO12RSB0
B41	IO09RSB0
B42	GND
B43	IO04RSB0
B44	IO01RSB0
C1	IO82RSB1
C2	IO79RSB1
C3	NC
C4	IO74RSB1
C5	GEA0/IO72RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO65RSB1
C10	IO62RSB1
C11	IO61RSB1
C12	IO58RSB1
C13	NC
C14	NC
C15	IO51RSB1
C16	VCCIB1

FG144



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG144	
Pin Number	**AGL125 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	**AGL125 Function**
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	**AGL125 Function**
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG484	
Pin Number	**AGL1000 Function**
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2

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