



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl1000v2-fg144i

Figure 1-5 • I/O States During Programming Window

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ²	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ²	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Applies to 1.2 V DC Core Voltage

Table 2-57 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
4 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
6 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
8 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
12 mA	Std.	1.55	3.85	0.26	0.98	1.10	3.91	3.53	3.24	3.77	9.69	9.32	ns
16 mA	Std.	1.55	3.69	0.26	0.98	1.10	3.75	3.44	3.28	3.84	9.54	9.23	ns
24 mA	Std.	1.55	3.61	0.26	0.98	1.10	3.67	3.46	3.33	4.13	9.45	9.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-58 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
4 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
6 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
8 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
12 mA	Std.	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
16 mA	Std.	1.55	2.63	0.26	0.98	1.10	2.67	2.14	3.28	4.01	8.45	7.93	ns
24 mA	Std.	1.55	2.65	0.26	0.98	1.10	2.69	2.10	3.33	4.31	8.47	7.89	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-59 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
4 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
6 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
8 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
12 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns
16 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-64 • Minimum and Maximum DC Input and Output Levels for LVC MOS 3.3 V Wide Range
Applicable to Standard Plus I/O Banks

3.3 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA ⁴	Max. mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < V_{\text{IN}} < V_{\text{IL}}$.
3. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{\text{IH}} < V_{\text{IN}} < V_{\text{CCI}}$. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

Table 2-113 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

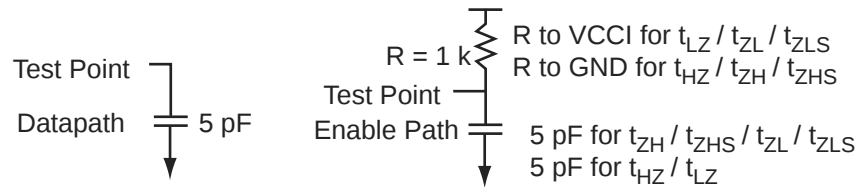


Figure 2-10 • AC Loading

Table 2-114 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-123 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.43	0.26	1.27	1.10	6.54	5.95	2.82	2.83	12.32	11.74	ns
4 mA	Std.	1.55	5.59	0.26	1.27	1.10	5.68	5.27	3.07	3.27	11.47	11.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-124 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.02	0.26	1.27	1.10	3.07	2.81	2.82	2.92	8.85	8.59	ns
4 mA	Std.	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-125 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.40	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-126 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-169 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	0.80	ns
AND2	$Y = A \cdot B$	t_{PD}	0.84	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.90	ns
OR2	$Y = A + B$	t_{PD}	1.19	ns
NOR2	$Y = !(A + B)$	t_{PD}	1.10	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.37	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	1.33	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.79	ns
MUX2	$Y = A !S + B S$	t_{PD}	1.48	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-170 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	1.34	ns
AND2	$Y = A \cdot B$	t_{PD}	1.43	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.59	ns
OR2	$Y = A + B$	t_{PD}	2.30	ns
NOR2	$Y = !(A + B)$	t_{PD}	2.07	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	2.46	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.12	ns
MUX2	$Y = A !S + B S$	t_{PD}	2.83	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-173 • AGL015 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-174 • AGL030 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Waveforms

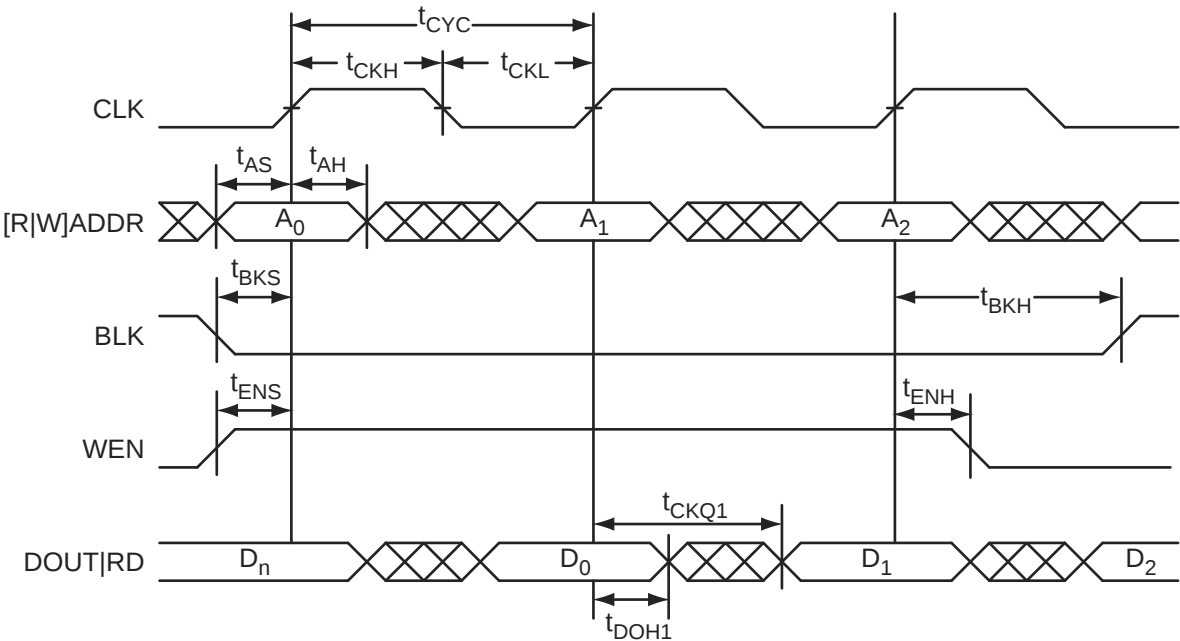


Figure 2-32 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

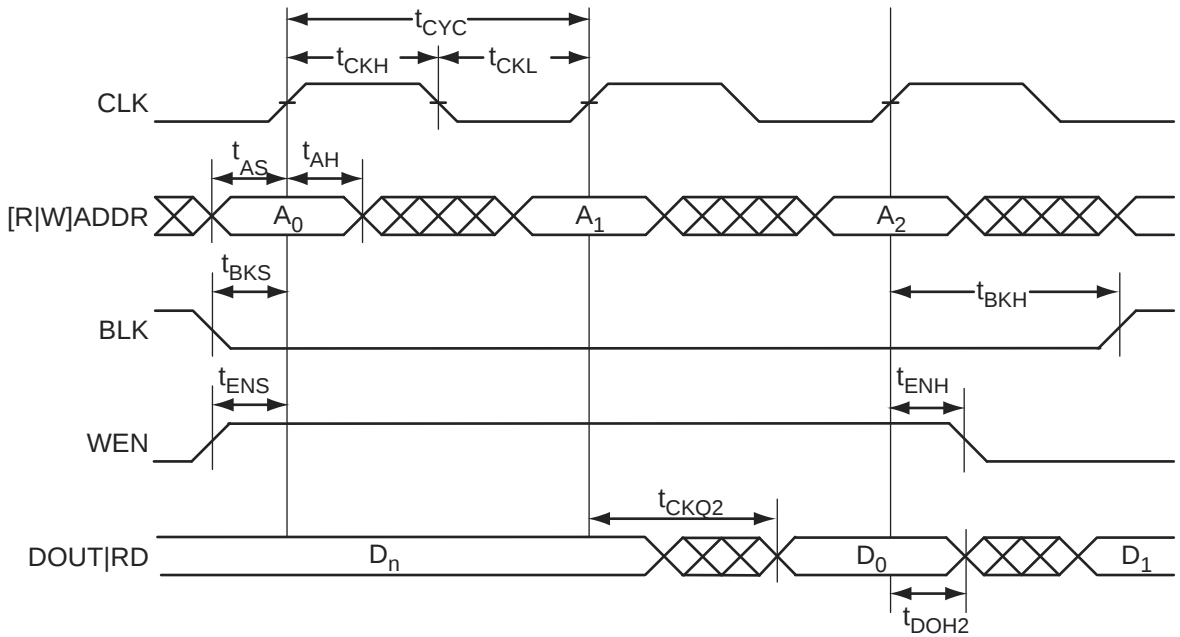


Figure 2-33 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

3 – Pin Descriptions

Supply Pins

GND**Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ**Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC**Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices, and 1.2 V or 1.5 V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx**I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx**I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F**PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

- 1.5 V for IGLOO V5 devices
- 1.2 V or 1.5 V for IGLOO V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

- There is one VCCPLF pin on IGLOO devices.

VCOMPLA/B/C/D/E/F**PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.

UC81	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

UC81	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

UC81	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

CS81	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS196	
Pin Number	AGL125 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	AGL125 Function
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	AGL125 Function
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

QN132	
Pin Number	AGL250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

VQ100	
Pin Number	AGL125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

VQ100	
Pin Number	AGL125 Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0

VQ100	
Pin Number	AGL125 Function
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

FG256	
Pin Number	AGL1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	AGL1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	AGL1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG484	
Pin Number	AGL600 Function
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	AGL600 Function
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

FG484	
Pin Number	AGL1000 Function
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO38RSB0
H12	IO47RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

FG484	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3