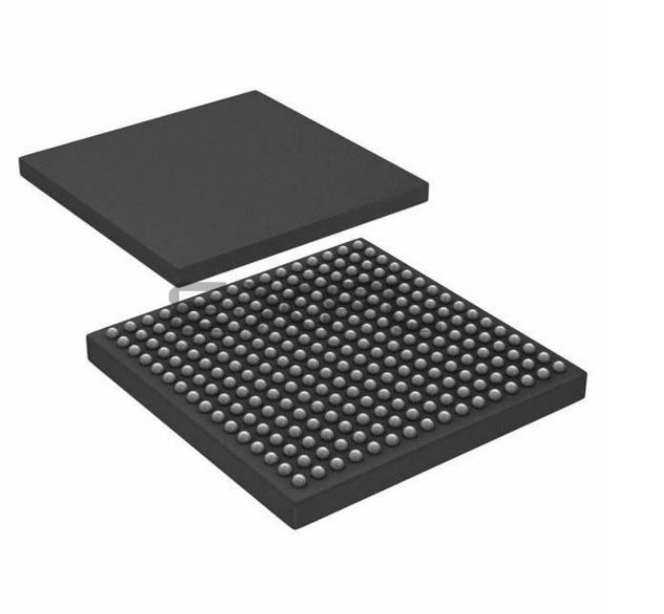

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl1000v2-fgg256i

IGLOO Ordering Information

AGL1000 V2 – FG G 144 Y I

- **I** — Application (Temperature Range)
  - Blank = Commercial (0°C to +85°C Junction Temperature)
  - I = Industrial (–40°C to +100°C Junction Temperature)
  - PP = Pre-Production
  - ES = Engineering Sample (Room Temperature Only)
- **Y** — Security Feature
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
  - Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- **144** — Package Lead Count
- **G** — Lead-Free Packaging
  - Blank = Standard Packaging
  - G= RoHS-Compliant Packaging (some packages also halogen-free)
- **FG** — Package Type
  - UC = Micro Chip Scale Package (0.4 mm pitch)
  - CS = Chip Scale Package (0.4 mm and 0.5 mm pitches)
  - QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitch)
  - VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
- **V2** — Supply Voltage
  - 2 = 1.2 V to 1.5 V
  - 5 = 1.5 V only
- **AGL1000** — Part Number

IGLOO Devices

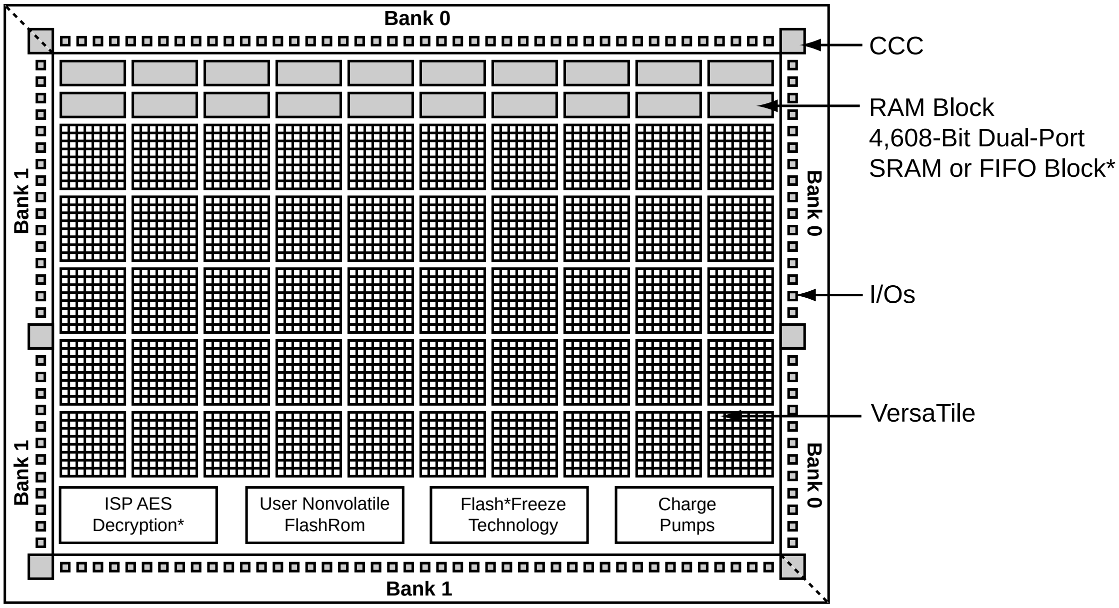
- AGL015 = 15,000 System Gates
- AGL030 = 30,000 System Gates
- AGL060 = 60,000 System Gates
- AGL125 = 125,000 System Gates
- AGL250 = 250,000 System Gates
- AGL400 = 400,000 System Gates
- AGL600 = 600,000 System Gates
- AGL1000 = 1,000,000 System Gates

IGLOO Devices with Cortex-M1

- M1AGL250 = 250,000 System Gates
- M1AGL600 = 600,000 System Gates
- M1AGL1000 = 1,000,000 System Gates

Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.



Note: *Not supported by AGL015 and AGL030 devices

Figure 1-1 • **IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)**

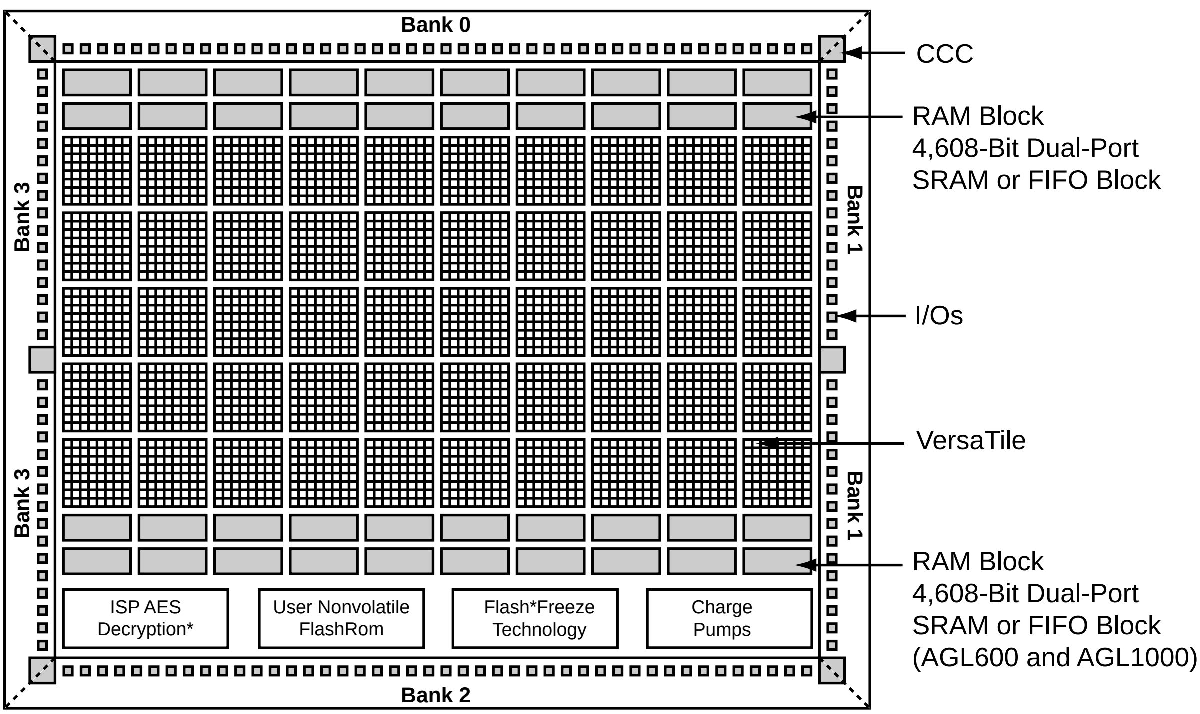


Figure 1-2 • **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)**

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V) For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.500	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.14 V) For IGLOO V2, 1.2 V DC Core Supply Voltage**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.967	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.874	0.885	0.894	0.899	0.902
1.26	0.794	0.803	0.814	0.821	0.827	0.830

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

	Power Supply Configurations				
Modes/power supplies	**VCC**	**VCCPLL**	**VCCI**	**VJTAG**	**VPUMP**
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	4	8	13	20	27	30	44	µA
	1.5 V	6	6	10	18	34	51	72	127	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microsemi Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24 on page 2-19. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25[2]	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[2]	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Detailed I/O DC Characteristics

Table 2-37 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-38 • **I/O Output Buffer Maximum Resistances[1] Applicable to Advanced I/O Banks**

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS[4]	2 mA	158	164
1.2 V LVCMOS Wide Range[4]	100 µA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL-DOWN-MAX)}$ = (VOLspec) / I_{OLspec}
3. $R_{(PULL-UP-MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}
4. *Applicable to IGLOO V2 Devices operating at VCCI ≥ VCC*

Table 2-42 • **I/O Short Currents IOSH/IOSL Applicable to Advanced I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *T_J = 100°C*

Table 2-77 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case VCCI = 2.7
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	4 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 µA	6 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns
100 µA	8 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-78 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	4 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 µA	6 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
100 µA	8 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

***Table 2-113* • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

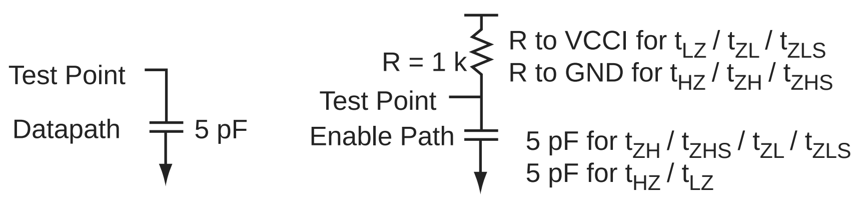


***Figure 2-10* • AC Loading**

***Table 2-114* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

***Table 2-123* • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.43	0.26	1.27	1.10	6.54	5.95	2.82	2.83	12.32	11.74	ns
4 mA	Std.	1.55	5.59	0.26	1.27	1.10	5.68	5.27	3.07	3.27	11.47	11.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-124* • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.02	0.26	1.27	1.10	3.07	2.81	2.82	2.92	8.85	8.59	ns
4 mA	Std.	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-125* • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.40	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-126* • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

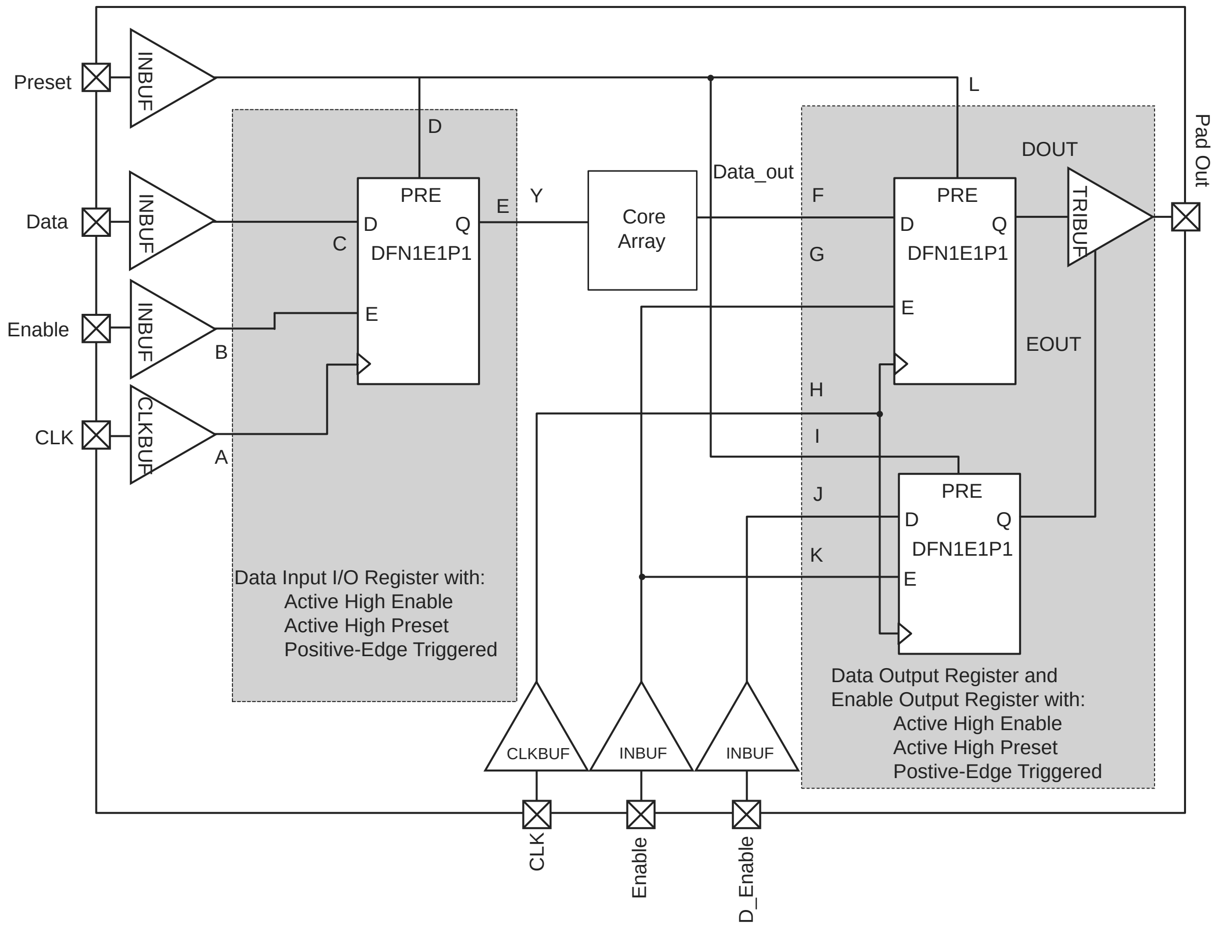


Figure 2-16 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-173* • AGL015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-174* • AGL030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Embedded FlashROM Characteristics

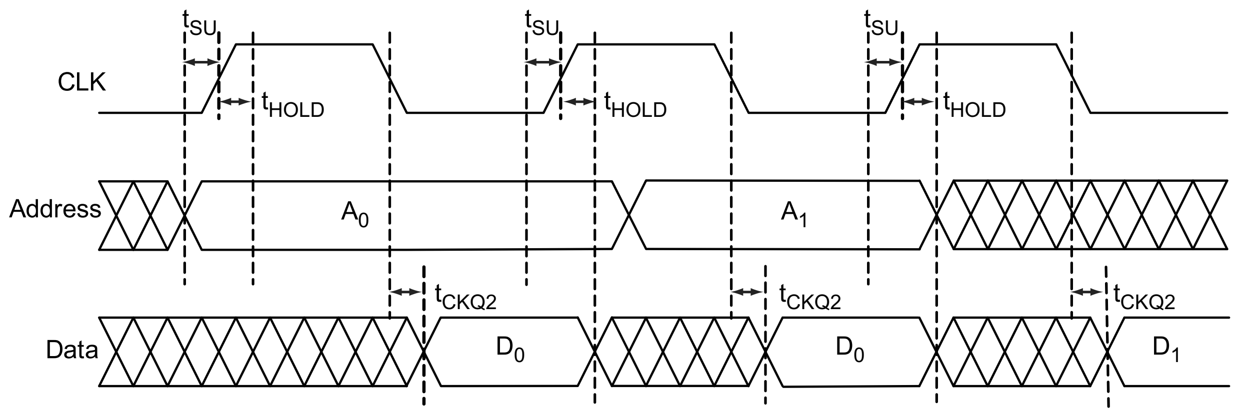


Figure 2-45 **• Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-197 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-198 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

CS281	
Pin Number	AGL600 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO07RSB0
A5	IO10RSB0
A6	IO14RSB0
A7	IO18RSB0
A8	IO21RSB0
A9	IO22RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO40RSB0
A13	IO37RSB0
A14	IO48RSB0
A15	IO51RSB0
A16	IO53RSB0
A17	GBC1/IO55RSB0
A18	GBA0/IO58RSB0
A19	GND
B1	GAA2/IO174PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO06RSB0
B6	GND
B7	IO15RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO24RSB0
B11	IO36RSB0
B12	IO35RSB0
B13	IO44RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO54RSB0
B17	GBA1/IO59RSB0

CS281	
Pin Number	AGL600 Function
B18	VCCIB1
B19	IO61NDB1
C1	GAB2/IO173PPB3
C2	IO174NPB3
C6	IO12RSB0
C14	IO50RSB0
C18	IO60NPB1
C19	GBB2/IO61PDB1
D1	IO170PPB3
D2	IO172NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO09RSB0
D7	IO16RSB0
D8	IO19RSB0
D9	IO26RSB0
D10	GND
D11	IO34RSB0
D12	IO45RSB0
D13	IO49RSB0
D14	IO47RSB0
D15	GBB0/IO56RSB0
D16	GBA2/IO60PPB1
D18	GBC2/IO62PPB1
D19	IO66NPB1
E1	IO169NPB3
E2	IO171PPB3
E4	IO171NPB3
E5	IO08RSB0
E6	IO11RSB0
E7	IO13RSB0
E8	IO17RSB0
E9	IO25RSB0
E10	IO30RSB0
E11	IO41RSB0
E12	IO42RSB0

CS281	
Pin Number	AGL600 Function
E13	IO46RSB0
E14	GBB1/IO57RSB0
E15	IO62NPB1
E16	IO63PPB1
E18	IO64PPB1
E19	IO65NPB1
F1	IO168NPB3
F2	GND
F3	IO169PPB3
F4	IO170NPB3
F5	IO173NPB3
F15	IO63NPB1
F16	IO65PPB1
F17	IO64NPB1
F18	GND
F19	IO68PPB1
G1	IO167NPB3
G2	IO165NDB3
G4	IO168PPB3
G5	IO167PPB3
G7	GAC2/IO172PPB3
G8	VCCIB0
G9	IO28RSB0
G10	IO32RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO66PPB1
G15	IO67NDB1
G16	IO67PDB1
G18	GCC0/IO69NPB1
G19	GCB1/IO70PPB1
H1	GFB0/IO163NPB3
H2	IO165PDB3
H4	GFC1/IO164PPB3
H5	GFB1/IO163PPB3
H7	VCCIB3

QN68	
Pin Number	**AGL030 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	**AGL030 Function**
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

FG256	
Pin Number	**AGL600 Function**
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

FG484	
Pin Number	**AGL400 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO15RSB0
A7	IO18RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO35RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO50RSB0
A17	IO51RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	NC
AA7	NC
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

FG484	
Pin Number	**AGL400 Function**
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	**AGL400 Function**
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1

FG484	
Pin Number	**AGL600 Function**
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2