Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

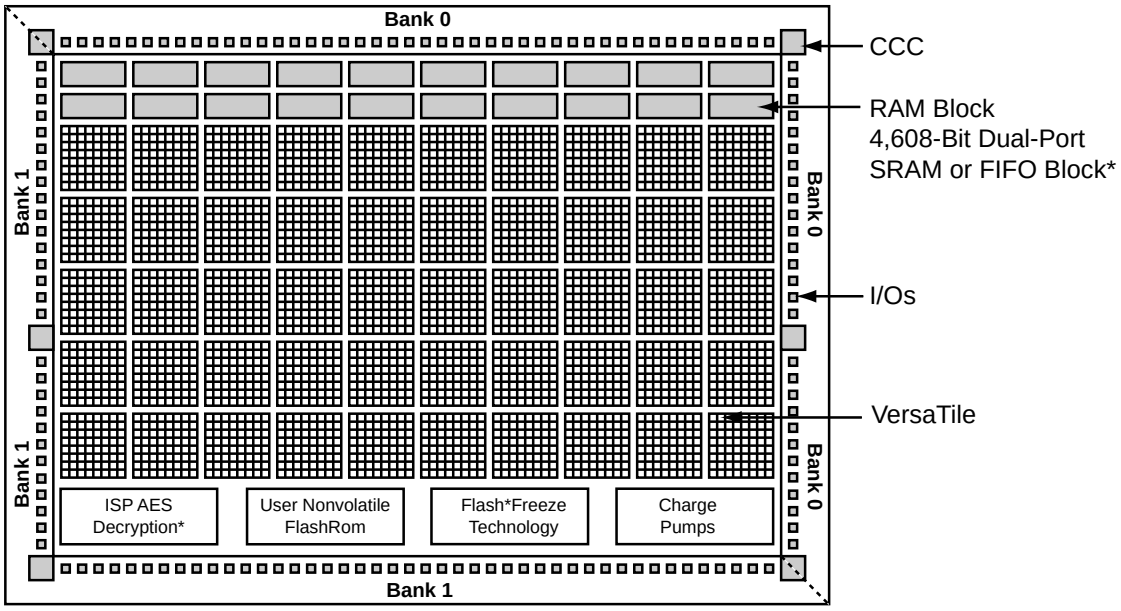
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 24576 |
| Total RAM Bits | 147456 |
| Number of I/O | 300 |
| Number of Gates | 1000000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1agl1000v2-fgg484i |

VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.




*Note: *Not supported by AGL015 and AGL030 devices*

***Figure 1-1 •*** **IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)**

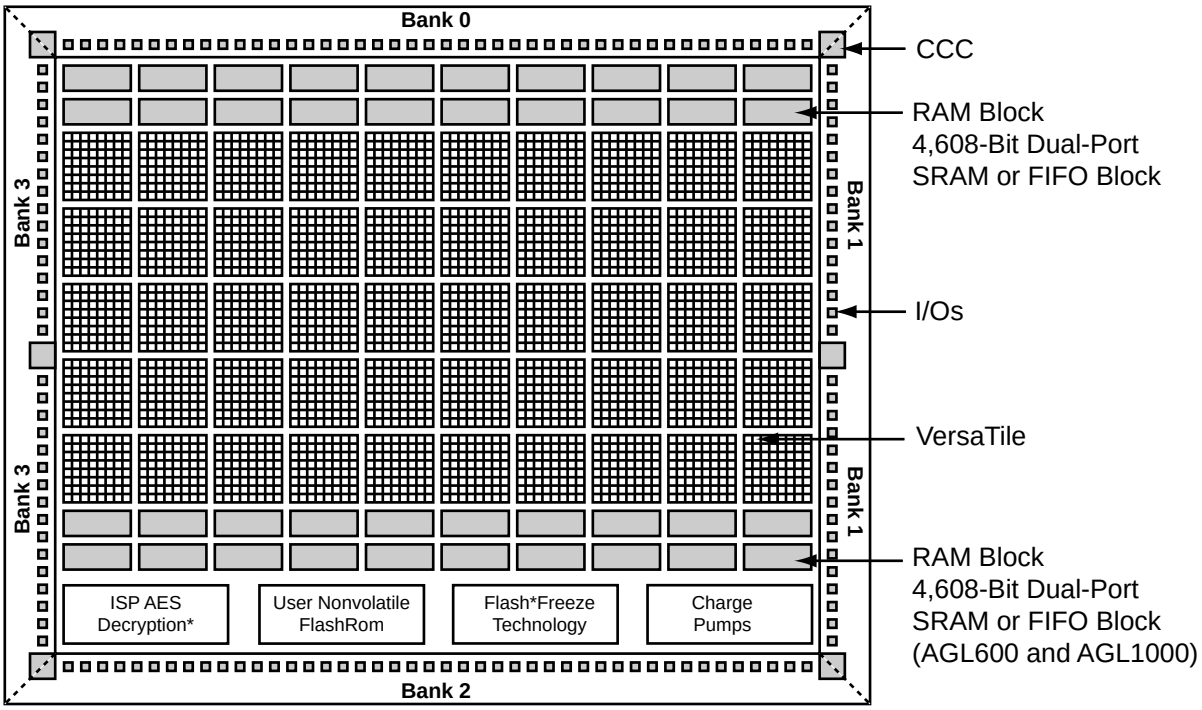



***Figure 1-2 •*** **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)**

## Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

***Table 2-3 •*** **Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

| Product Grade | Programming Cycles | Program Retention (biased/unbiased) | Maximum Storage Temperature $T_{STG}$ (°C) [2] | Maximum Operating Junction Temperature $T_J$ (°C) [2] |
|---|---|---|---|---|
| Commercial | 500 | 20 years | 110 | 100 |
| Industrial | 500 | 20 years | 110 | 100 |

*Notes:*

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 on page 2-2 for device operating conditions and absolute limits.*

***Table 2-4 •*** **Overshoot and Undershoot Limits [1]**

| VCCI | Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7 V or less | 10% | 1.4 V |
| | 5% | 1.49 V |
| 3 V | 10% | 1.1 V |
| | 5% | 1.19 V |
| 3.3 V | 10% | 0.79 V |
| | 5% | 0.88 V |
| 3.6 V | 10% | 0.45 V |
| | 5% | 0.54 V |

*Notes:*

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

**V**CCI **Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 Devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

**V**CC **Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

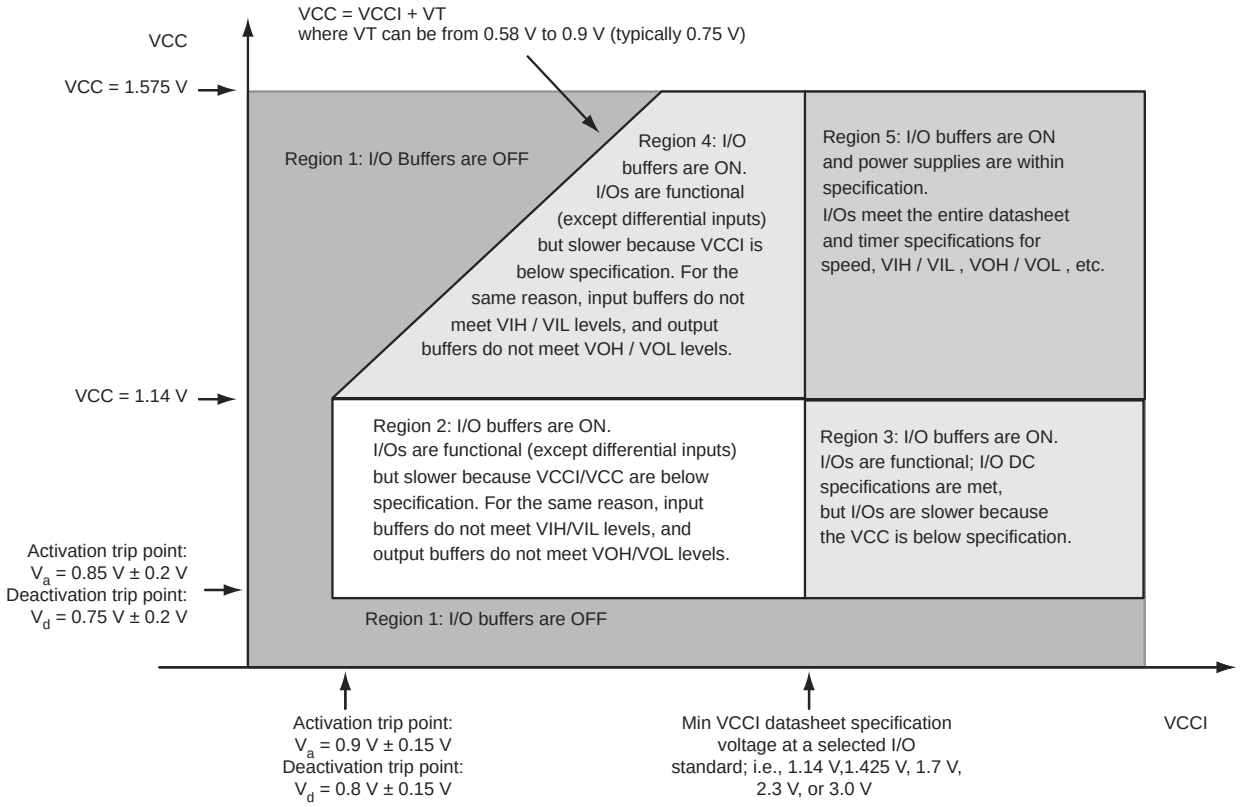



***Figure 2-2 •*** **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

# Thermal Characteristics

## *Introduction*

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

*EQ 1*

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

## Power per I/O Pin

***Table 2-13 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks**

| | VCCI (V) | Static Power PDC6 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | – | 16.27 |
| 3.3 V LVCMOS Wide Range[3] | 3.3 | – | 16.27 |
| 2.5 V LVCMOS | 2.5 | – | 4.65 |
| 1.8 V LVCMOS | 1.8 | – | 1.61 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 0.96 |
| 1.2 V LVCMOS[4] | 1.2 | – | 0.58 |
| 1.2 V LVCMOS Wide Range[4] | 1.2 | – | 0.58 |
| 3.3 V PCI | 3.3 | – | 17.67 |
| 3.3 V PCI-X | 3.3 | – | 17.67 |
| **Differential** | | | |
| LVDS | 2.5 | 2.26 | 23.39 |
| LVPECL | 3.3 | 5.72 | 59.05 |

*Notes:*

1. *$P_{DC6}$ is the static power (where applicable) measured on VCCI.*
2. *$P_{AC9}$ is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO V2 devices only*

***Table 2-14 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

| | VCCI (V) | Static Power PDC6 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | – | 16.41 |
| 3.3 V LVCMOS Wide Range[3] | 3.3 | – | 16.41 |
| 2.5 V LVCMOS | 2.5 | – | 4.75 |
| 1.8 V LVCMOS | 1.8 | – | 1.66 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.00 |
| 1.2 V LVCMOS[4] | 1.2 | – | 0.61 |
| 1.2 V LVCMOS Wide Range[4] | 1.2 | – | 0.61 |
| 3.3 V PCI | 3.3 | – | 17.78 |
| 3.3 V PCI-X | 3.3 | – | 17.78 |

*Notes:*

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *Applicable for IGLOO V2 devices only.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

# User I/O Characteristics

## Timing Model

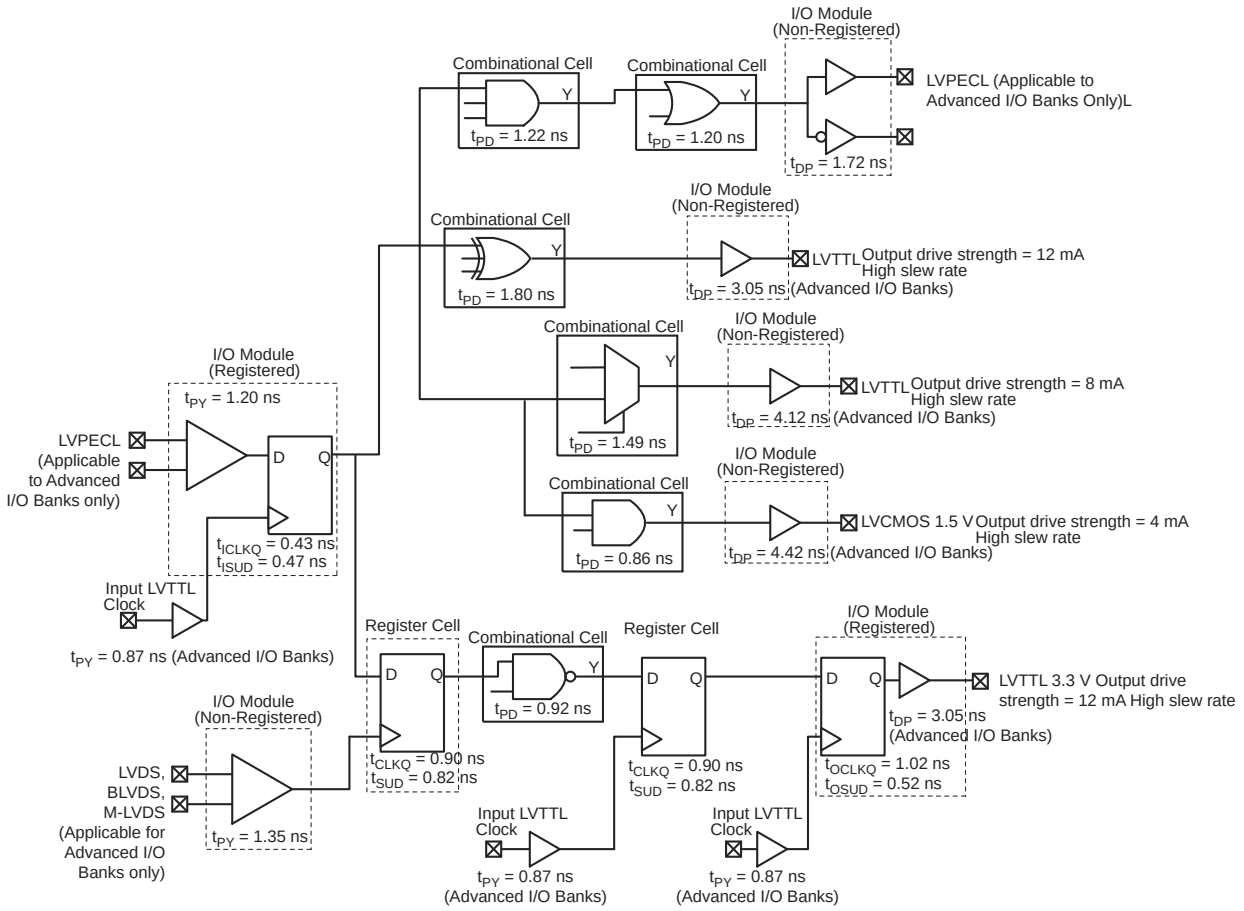



***Figure 2-3 •*** **Timing Model**
**Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices**

**Table 2-42 • I/O Short Currents IOSH/IOSL**
**Applicable to Advanced I/O Banks**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 132 | 127 |
| | 24 mA | 268 | 181 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| | 16 mA | 83 | 87 |
| | 24 mA | 169 | 124 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 45 | 51 |
| | 12 mA | 91 | 74 |
| | 16 mA | 91 | 74 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| | 6 mA | 32 | 39 |
| | 8 mA | 66 | 55 |
| | 12 mA | 66 | 55 |
| 1.2 V LVCMOS | 2 mA | 20 | 26 |
| 1.2 V LVCMOS Wide Range | 100 µA | 20 | 26 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 103 | 109 |

*Note: *$T_J$ = 100°C*

***Applies to 1.2 V DC Core Voltage***

***Table 2-73 •*** **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 V**
**Applicable to Advanced Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 1.55 | 7.52 | 0.26 | 1.32 | 1.10 | 7.52 | 6.38 | 3.84 | 4.02 | 13.31 | 12.16 | ns |
| 100 µA | 4 mA | Std. | 1.55 | 7.52 | 0.26 | 1.32 | 1.10 | 7.52 | 6.38 | 3.84 | 4.02 | 13.31 | 12.16 | ns |
| 100 µA | 6 mA | Std. | 1.55 | 6.37 | 0.26 | 1.32 | 1.10 | 6.37 | 5.57 | 4.23 | 4.73 | 12.16 | 11.35 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 6.37 | 0.26 | 1.32 | 1.10 | 6.37 | 5.57 | 4.23 | 4.73 | 12.16 | 11.35 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 5.55 | 0.26 | 1.32 | 1.10 | 5.55 | 4.96 | 4.50 | 5.18 | 11.34 | 10.75 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 5.32 | 0.26 | 1.32 | 1.10 | 5.32 | 4.82 | 4.56 | 5.29 | 11.10 | 10.61 | ns |
| 100 µA | 24 mA | Std. | 1.55 | 5.19 | 0.26 | 1.32 | 1.10 | 5.19 | 4.85 | 4.63 | 5.74 | 10.98 | 10.63 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-74 •*** **3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7**
**Applicable to Advanced Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 1.55 | 4.75 | 0.26 | 1.32 | 1.10 | 4.75 | 3.77 | 3.84 | 4.27 | 10.54 | 9.56 | ns |
| 100 µA | 4 mA | Std. | 1.55 | 4.75 | 0.26 | 1.32 | 1.10 | 4.75 | 3.77 | 3.84 | 4.27 | 10.54 | 9.56 | ns |
| 100 µA | 6 mA | Std. | 1.55 | 4.10 | 0.26 | 1.32 | 1.10 | 4.10 | 3.19 | 4.24 | 4.98 | 9.88 | 8.98 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 4.10 | 0.26 | 1.32 | 1.10 | 4.10 | 3.19 | 4.24 | 4.98 | 9.88 | 8.98 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 3.73 | 0.26 | 1.32 | 1.10 | 3.73 | 2.91 | 4.51 | 5.43 | 9.52 | 8.69 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 3.67 | 0.26 | 1.32 | 1.10 | 3.67 | 2.85 | 4.57 | 5.55 | 9.46 | 8.64 | ns |
| 100 µA | 24 mA | Std. | 1.55 | 3.70 | 0.26 | 1.32 | 1.10 | 3.70 | 2.79 | 4.65 | 6.01 | 9.49 | 8.58 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

***Table 2-81 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

| 2.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | 2 | 16 | 18 | 10 | 10 |
| 4 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 4 | 4 | 16 | 18 | 10 | 10 |
| 6 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 6 | 6 | 32 | 37 | 10 | 10 |
| 8 mA | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 32 | 37 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

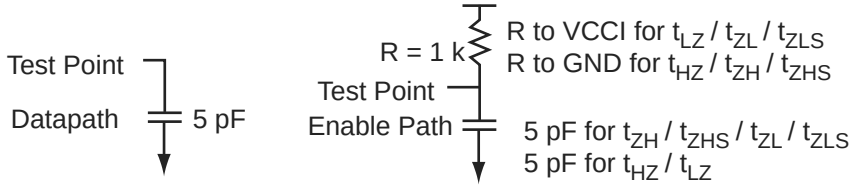



***Figure 2-8 •*** **AC Loading**

***Table 2-82 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 2.5 | 1.2 | 5 |

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

***Table 2-156 •*** **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

*Note: *See Figure 2-17 on page 2-86 for more information.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

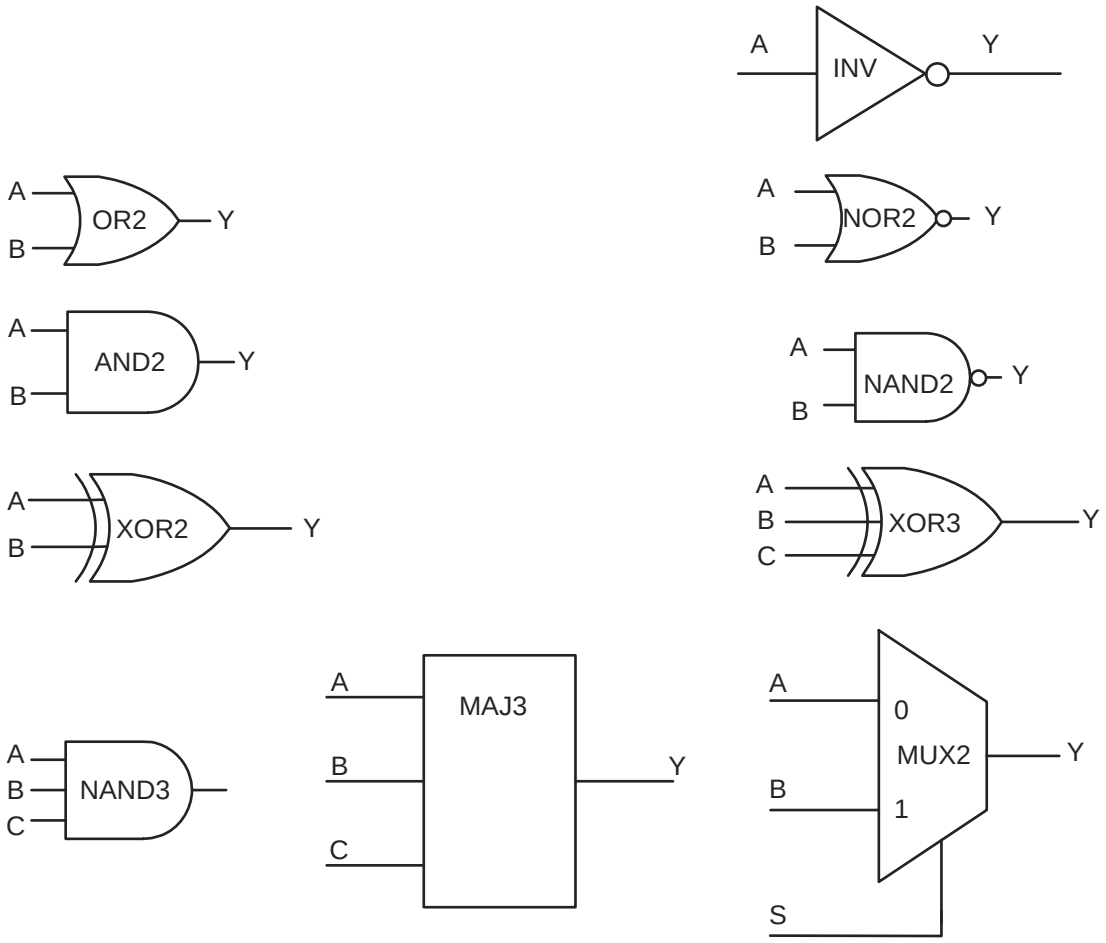


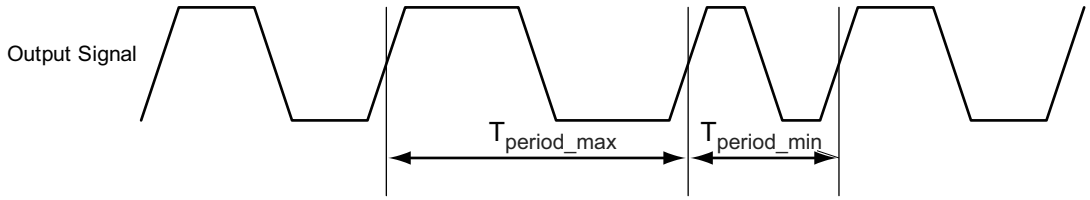

***Figure 2-25 •*** **Sample of Combinatorial Cells**

***Table 2-190 •*** **IGLOO CCC/PLL Specification**
**For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | 1.5 | | 160 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | 0.75 | | 160 | MHz |
| Delay Increments in Programmable Delay Blocks [1, 2] | | 580[3] | | ps |
| Number of Programmable Values in Each Programmable Delay Block | | | 32 | |
| Serial Clock (SCLK) for Dynamic PLL[4,5] | | | 60 | ns |
| Input Cycle-to-Cycle Jitter (peak magnitude) | | | 0.25 | ns |
| Acquisition Time | | | | |
| LockControl = 0 | | | 300 | µs |
| LockControl = 1 | | | 6.0 | ms |
| Tracking Jitter[6] | | | | |
| LockControl = 0 | | | 4 | ns |
| LockControl = 1 | | | 3 | ns |
| Output Duty Cycle | 48.5 | | 51.5 | % |
| Delay Range in Block: Programmable Delay 1[1,2] | 2.3 | | 20.86 | ns |
| Delay Range in Block: Programmable Delay 2[1,2] | 0.863 | | 20.86 | ns |
| Delay Range in Block: Fixed Delay [1, 2, 5] | | 5.7 | | ns |
| CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ | Maximum Peak-to-Peak Jitter Data[7,8] | | | |
| | SSO ≥ 4[9] | SSO ≥ 8[9] | SSO ≥ 16[9] | |
| 0.75 MHz to 50 MHz | 1.20% | 2.00% | 3.00% | |
| 50 MHz to 160 MHz | 5.00% | 7.00% | 15.00% | |

*Notes:*

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.*
2. *$T_J$ = 25°C, $V_{CC}$ = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
5. *The AGL030 device does not support a PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.*
10. *For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the IGLOO FPGA Fabric User Guide.*




*Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} – T_{period\_min}$.*

***Figure 2-30 •*** **Peak-to-Peak Jitter Definition**

# JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

## *Timing Characteristics*

***Table 2-199 •*** **JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.00 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 2.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.00 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 2.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 25.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 15 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-200 •*** **JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.50 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 3.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.50 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 3.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 11.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 30.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| A1 | GND |
| A2 | GAB0/IO02RSB0 |
| A3 | GAC1/IO05RSB0 |
| A4 | IO07RSB0 |
| A5 | IO10RSB0 |
| A6 | IO14RSB0 |
| A7 | IO18RSB0 |
| A8 | IO21RSB0 |
| A9 | IO22RSB0 |
| A10 | VCCIB0 |
| A11 | IO33RSB0 |
| A12 | IO40RSB0 |
| A13 | IO37RSB0 |
| A14 | IO48RSB0 |
| A15 | IO51RSB0 |
| A16 | IO53RSB0 |
| A17 | GBC1/IO55RSB0 |
| A18 | GBA0/IO58RSB0 |
| A19 | GND |
| B1 | GAA2/IO174PPB3 |
| B2 | VCCIB0 |
| B3 | GAB1/IO03RSB0 |
| B4 | GAC0/IO04RSB0 |
| B5 | IO06RSB0 |
| B6 | GND |
| B7 | IO15RSB0 |
| B8 | IO20RSB0 |
| B9 | IO23RSB0 |
| B10 | IO24RSB0 |
| B11 | IO36RSB0 |
| B12 | IO35RSB0 |
| B13 | IO44RSB0 |
| B14 | GND |
| B15 | IO52RSB0 |
| B16 | GBC0/IO54RSB0 |
| B17 | GBA1/IO59RSB0 |

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| B18 | VCCIB1 |
| B19 | IO61NDB1 |
| C1 | GAB2/IO173PPB3 |
| C2 | IO174NPB3 |
| C6 | IO12RSB0 |
| C14 | IO50RSB0 |
| C18 | IO60NPB1 |
| C19 | GBB2/IO61PDB1 |
| D1 | IO170PPB3 |
| D2 | IO172NPB3 |
| D4 | GAA0/IO00RSB0 |
| D5 | GAA1/IO01RSB0 |
| D6 | IO09RSB0 |
| D7 | IO16RSB0 |
| D8 | IO19RSB0 |
| D9 | IO26RSB0 |
| D10 | GND |
| D11 | IO34RSB0 |
| D12 | IO45RSB0 |
| D13 | IO49RSB0 |
| D14 | IO47RSB0 |
| D15 | GBB0/IO56RSB0 |
| D16 | GBA2/IO60PPB1 |
| D18 | GBC2/IO62PPB1 |
| D19 | IO66NPB1 |
| E1 | IO169NPB3 |
| E2 | IO171PPB3 |
| E4 | IO171NPB3 |
| E5 | IO08RSB0 |
| E6 | IO11RSB0 |
| E7 | IO13RSB0 |
| E8 | IO17RSB0 |
| E9 | IO25RSB0 |
| E10 | IO30RSB0 |
| E11 | IO41RSB0 |
| E12 | IO42RSB0 |

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| E13 | IO46RSB0 |
| E14 | GBB1/IO57RSB0 |
| E15 | IO62NPB1 |
| E16 | IO63PPB1 |
| E18 | IO64PPB1 |
| E19 | IO65NPB1 |
| F1 | IO168NPB3 |
| F2 | GND |
| F3 | IO169PPB3 |
| F4 | IO170NPB3 |
| F5 | IO173NPB3 |
| F15 | IO63NPB1 |
| F16 | IO65PPB1 |
| F17 | IO64NPB1 |
| F18 | GND |
| F19 | IO68PPB1 |
| G1 | IO167NPB3 |
| G2 | IO165NDB3 |
| G4 | IO168PPB3 |
| G5 | IO167PPB3 |
| G7 | GAC2/IO172PPB3 |
| G8 | VCCIB0 |
| G9 | IO28RSB0 |
| G10 | IO32RSB0 |
| G11 | IO43RSB0 |
| G12 | VCCIB0 |
| G13 | IO66PPB1 |
| G15 | IO67NDB1 |
| G16 | IO67PDB1 |
| G18 | GCC0/IO69NPB1 |
| G19 | GCB1/IO70PPB1 |
| H1 | GFB0/IO163NPB3 |
| H2 | IO165PDB3 |
| H4 | GFC1/IO164PPB3 |
| H5 | GFB1/IO163PPB3 |
| H7 | VCCIB3 |

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| H8 | VCC |
| H9 | VCCIB0 |
| H10 | VCC |
| H11 | VCCIB0 |
| H12 | VCC |
| H13 | VCCIB1 |
| H15 | IO68NPB1 |
| H16 | GCB0/IO70NPB1 |
| H18 | GCA1/IO71PPB1 |
| H19 | GCA2/IO72PPB1 |
| J1 | VCOMPLF |
| J2 | GFA0/IO162NDB3 |
| J4 | VCCPLF |
| J5 | GFC0/IO164NPB3 |
| J7 | GFA2/IO161PDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | GND |
| J11 | GND |
| J12 | VCCIB1 |
| J13 | GCC1/IO69PPB1 |
| J15 | GCA0/IO71NPB1 |
| J16 | GCB2/IO73PPB1 |
| J18 | IO72NPB1 |
| J19 | IO75PSB1 |
| K1 | VCCIB3 |
| K2 | GFA1/IO162PDB3 |
| K4 | GND |
| K5 | IO159NPB3 |
| K7 | IO161NDB3 |
| K8 | VCC |
| K9 | GND |
| K10 | GND |
| K11 | GND |
| K12 | VCC |
| K13 | GCC2/IO74PPB1 |

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| K15 | IO73NPB1 |
| K16 | GND |
| K18 | IO74NPB1 |
| K19 | VCCIB1 |
| L1 | GFB2/IO160PDB3 |
| L2 | IO160NDB3 |
| L4 | GFC2/IO159PPB3 |
| L5 | IO153PPB3 |
| L7 | IO153NPB3 |
| L8 | VCCIB3 |
| L9 | GND |
| L10 | GND |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | IO76PPB1 |
| L15 | IO76NPB1 |
| L16 | IO77PPB1 |
| L18 | IO78NPB1 |
| L19 | IO77NPB1 |
| M1 | IO158PDB3 |
| M2 | IO158NDB3 |
| M4 | IO154NPB3 |
| M5 | IO152PPB3 |
| M7 | VCCIB3 |
| M8 | VCC |
| M9 | VCCIB2 |
| M10 | VCC |
| M11 | VCCIB2 |
| M12 | VCC |
| M13 | VCCIB1 |
| M15 | IO79NPB1 |
| M16 | IO81NPB1 |
| M18 | IO79PPB1 |
| M19 | IO78PPB1 |
| N1 | IO154PPB3 |
| N2 | IO152NPB3 |

| CS281 | |
|---|---|
| Pin Number | AGL600 Function |
| N4 | IO150PPB3 |
| N5 | IO148NPB3 |
| N7 | GEA2/IO143RSB2 |
| N8 | VCCIB2 |
| N9 | IO117RSB2 |
| N10 | IO115RSB2 |
| N11 | IO114RSB2 |
| N12 | VCCIB2 |
| N13 | VPUMP |
| N15 | IO82PPB1 |
| N16 | IO85PPB1 |
| N18 | IO82NPB1 |
| N19 | IO81PPB1 |
| P1 | IO151PDB3 |
| P2 | GND |
| P3 | IO151NDB3 |
| P4 | IO149PPB3 |
| P5 | GEA0/IO144NPB3 |
| P15 | IO83NDB1 |
| P16 | IO83PDB1 |
| P17 | GDC1/IO86PPB1 |
| P18 | GND |
| P19 | IO85NPB1 |
| R1 | IO150NPB3 |
| R2 | IO149NPB3 |
| R4 | GEC1/IO146PPB3 |
| R5 | GEB1/IO145PPB3 |
| R6 | IO138RSB2 |
| R7 | IO127RSB2 |
| R8 | IO123RSB2 |
| R9 | IO118RSB2 |
| R10 | IO111RSB2 |
| R11 | IO106RSB2 |
| R12 | IO103RSB2 |
| R13 | IO97RSB2 |
| R14 | IO95RSB2 |

| QN48 | |
|---|---|
| **Pin Number** | **AGL030 Function** |
| 1 | IO82RSB1 |
| 2 | GEC0/IO73RSB1 |
| 3 | GEA0/IO72RSB1 |
| 4 | GEB0/IO71RSB1 |
| 5 | GND |
| 6 | VCCIB1 |
| 7 | IO68RSB1 |
| 8 | IO67RSB1 |
| 9 | IO66RSB1 |
| 10 | IO65RSB1 |
| 11 | IO64RSB1 |
| 12 | IO62RSB1 |
| 13 | IO61RSB1 |
| 14 | FF/IO60RSB1 |
| 15 | IO57RSB1 |
| 16 | IO55RSB1 |
| 17 | IO53RSB1 |
| 18 | VCC |
| 19 | VCCIB1 |
| 20 | IO46RSB1 |
| 21 | IO42RSB1 |
| 22 | TCK |
| 23 | TDI |
| 24 | TMS |
| 25 | VPUMP |
| 26 | TDO |
| 27 | TRST |
| 28 | VJTAG |
| 29 | IO38RSB0 |
| 30 | GDB0/IO34RSB0 |
| 31 | GDA0/IO33RSB0 |
| 32 | GDC0/IO32RSB0 |
| 33 | VCCIB0 |
| 34 | GND |
| 35 | VCC |
| 36 | IO25RSB0 |

| QN48 | |
|---|---|
| **Pin Number** | **AGL030 Function** |
| 37 | IO24RSB0 |
| 38 | IO22RSB0 |
| 39 | IO20RSB0 |
| 40 | IO18RSB0 |
| 41 | IO16RSB0 |
| 42 | IO14RSB0 |
| 43 | IO10RSB0 |
| 44 | IO08RSB0 |
| 45 | IO06RSB0 |
| 46 | IO04RSB0 |
| 47 | IO02RSB0 |
| 48 | IO00RSB0 |

| FG256 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| H3 | GFB1/IO163PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO164NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO69NPB1 |
| H13 | GCB1/IO70PPB1 |
| H14 | GCA0/IO71NPB1 |
| H15 | IO67NPB1 |
| H16 | GCB0/IO70NPB1 |
| J1 | GFA2/IO161PPB3 |
| J2 | GFA1/IO162PDB3 |
| J3 | VCCPLF |
| J4 | IO160NDB3 |
| J5 | GFB2/IO160PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO73PPB1 |
| J13 | GCA1/IO71PPB1 |
| J14 | GCC2/IO74PPB1 |
| J15 | IO80PPB1 |
| J16 | GCA2/IO72PDB1 |
| K1 | GFC2/IO159PDB3 |
| K2 | IO161NPB3 |
| K3 | IO156PPB3 |
| K4 | IO129RSB2 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |

| FG256 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO73NPB1 |
| K14 | IO80NPB1 |
| K15 | IO74NPB1 |
| K16 | IO72NDB1 |
| L1 | IO159NDB3 |
| L2 | IO156NPB3 |
| L3 | IO151PPB3 |
| L4 | IO158PSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO87NPB1 |
| L14 | IO85NDB1 |
| L15 | IO85PDB1 |
| L16 | IO84PDB1 |
| M1 | IO150PDB3 |
| M2 | IO151NPB3 |
| M3 | IO147NPB3 |
| M4 | GEC0/IO146NPB3 |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO117RSB2 |
| M9 | IO110RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO94RSB2 |
| M14 | GDB1/IO87PPB1 |

| FG256 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| M15 | GDC1/IO86PDB1 |
| M16 | IO84NDB1 |
| N1 | IO150NDB3 |
| N2 | IO147PPB3 |
| N3 | GEC1/IO146PPB3 |
| N4 | IO140RSB2 |
| N5 | GNDQ |
| N6 | GEA2/IO143RSB2 |
| N7 | IO126RSB2 |
| N8 | IO120RSB2 |
| N9 | IO108RSB2 |
| N10 | IO103RSB2 |
| N11 | IO99RSB2 |
| N12 | GNDQ |
| N13 | IO92RSB2 |
| N14 | VJTAG |
| N15 | GDC0/IO86NDB1 |
| N16 | GDA1/IO88PDB1 |
| P1 | GEB1/IO145PDB3 |
| P2 | GEB0/IO145NDB3 |
| P3 | VMV2 |
| P4 | IO138RSB2 |
| P5 | IO136RSB2 |
| P6 | IO131RSB2 |
| P7 | IO124RSB2 |
| P8 | IO119RSB2 |
| P9 | IO107RSB2 |
| P10 | IO104RSB2 |
| P11 | IO97RSB2 |
| P12 | VMV1 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO88NDB1 |
| R1 | GEA1/IO144PDB3 |
| R2 | GEA0/IO144NDB3 |
| R3 | IO139RSB2 |
| R4 | GEC2/IO141RSB2 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| V15 | IO85RSB2 |
| V16 | GDB2/IO81RSB2 |
| V17 | TDI |
| V18 | NC |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | NC |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO126RSB2 |
| W6 | FF/GEB2/IO133RSB2 |
| W7 | IO124RSB2 |
| W8 | IO116RSB2 |
| W9 | IO113RSB2 |
| W10 | IO107RSB2 |
| W11 | IO105RSB2 |
| W12 | IO102RSB2 |
| W13 | IO97RSB2 |
| W14 | IO92RSB2 |
| W15 | GDC2/IO82RSB2 |
| W16 | IO86RSB2 |
| W17 | GDA2/IO80RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB3 |
| Y2 | NC |
| Y3 | NC |
| Y4 | NC |
| Y5 | GND |
| Y6 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |
| D7 | GAB0/IO02RSB0 |
| D8 | IO11RSB0 |
| D9 | IO16RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | IO34RSB0 |
| D13 | IO37RSB0 |
| D14 | IO41RSB0 |
| D15 | IO43RSB0 |
| D16 | GBB1/IO57RSB0 |
| D17 | GBA0/IO58RSB0 |
| D18 | GBA1/IO59RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | NC |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO173PDB3 |
| E5 | GAA2/IO174PDB3 |
| E6 | GNDQ |
| E7 | GAB1/IO03RSB0 |
| E8 | IO13RSB0 |
| E9 | IO14RSB0 |
| E10 | IO21RSB0 |
| E11 | IO27RSB0 |
| E12 | IO32RSB0 |