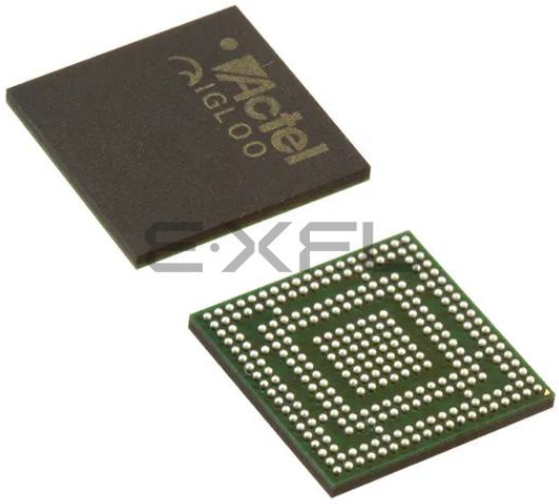

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	215
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl1000v5-csg281i

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • **I/O Standards Supported**

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west banks of AGL250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of AGL250 and larger devices All banks of AGL060 and AGL125K	✓	✓	Not supported
Standard	All banks of AGL015 and AGL030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range[3]	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.64
1.8 V LVCMOS	1.8	–	2.63
1.5 V LVCMOS (JESD8-11)	1.5	–	1.97
1.2 V LVCMOS[4]	1.2	–	0.57
1.2 V LVCMOS Wide Range[4]	1.2	–	0.57

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO V2 devices only.*

Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	136.95
3.3 V LVCMOS Wide Range[4]	5	3.3	–	136.95
2.5 V LVCMOS	5	2.5	–	76.84
1.8 V LVCMOS	5	1.8	–	49.31
1.5 V LVCMOS (JESD8-11)	5	1.5	–	33.36
1.2 V LVCMOS[5]	5	1.2	–	16.24
1.2 V LVCMOS Wide Range[5]	5	1.2	–	16.24
3.3 V PCI	10	3.3	–	194.05
3.3 V PCI-X	10	3.3	–	194.05
Differential				
LVDS	–	2.5	7.74	156.22
LVPECL	–	3.3	19.54	339.35

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
5. *Applicable for IGLOO V2 devices only.*

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.†

† *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-42 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

*Note: *T_J = 100°C*

***Table 2-151* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

***Table 2-152* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

*Note: *Measuring point = Vtrip. See Table 2-28 on page 2-104 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-153* • LVPECL – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

***Table 2-154* • LVPECL – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-165 • Input DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

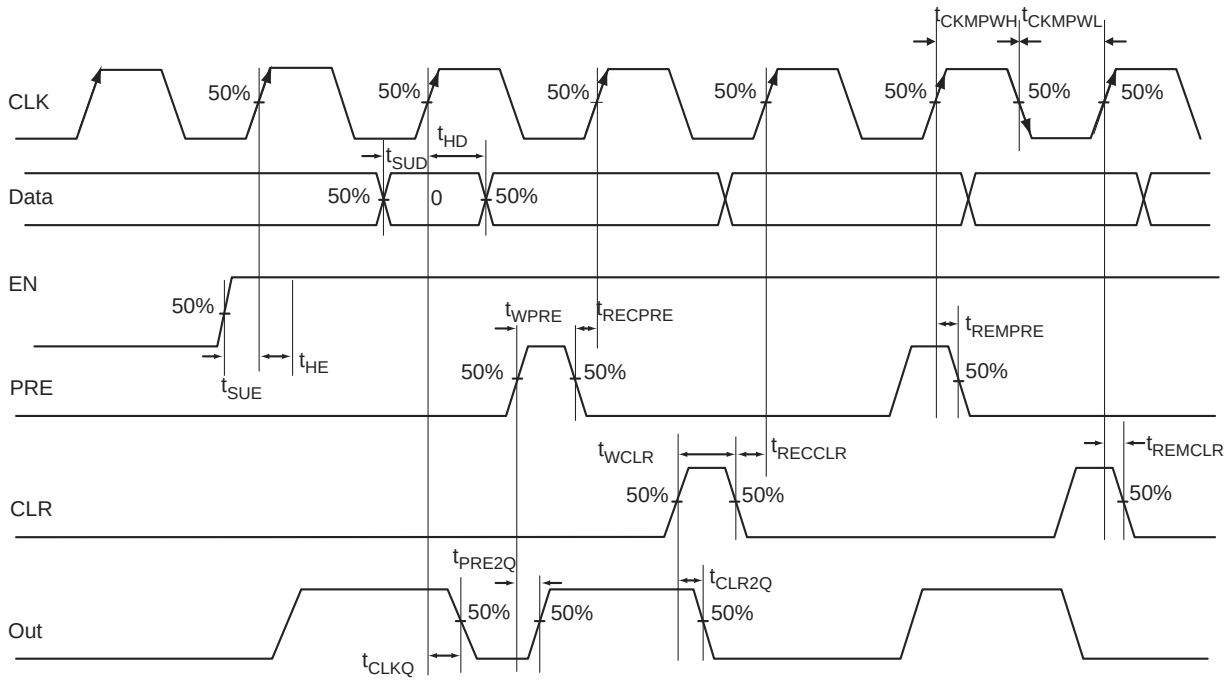


Figure 2-28 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-171 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-177 • **AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-178 • **AGL400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min. [1]	Max. [2]	
t_{RCKL}	Input Low Delay for Global Clock	1.45	1.79	ns
t_{RCKH}	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-190 • **IGLOO CCC/PLL Specification**
For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1[1,2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2[1,2]	0.863		20.86	ns
Delay Range in Block: Fixed Delay [1, 2, 5]		5.7		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7,8]			
	SSO ≥ 4[9]	SSO ≥ 8[9]	SSO ≥ 16[9]	
0.75 MHz to 50 MHz	1.20%	2.00%	3.00%	
50 MHz to 160 MHz	5.00%	7.00%	15.00%	

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
5. *The AGL030 device does not support a PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.*
10. *For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the IGLOO FPGA Fabric User Guide.*

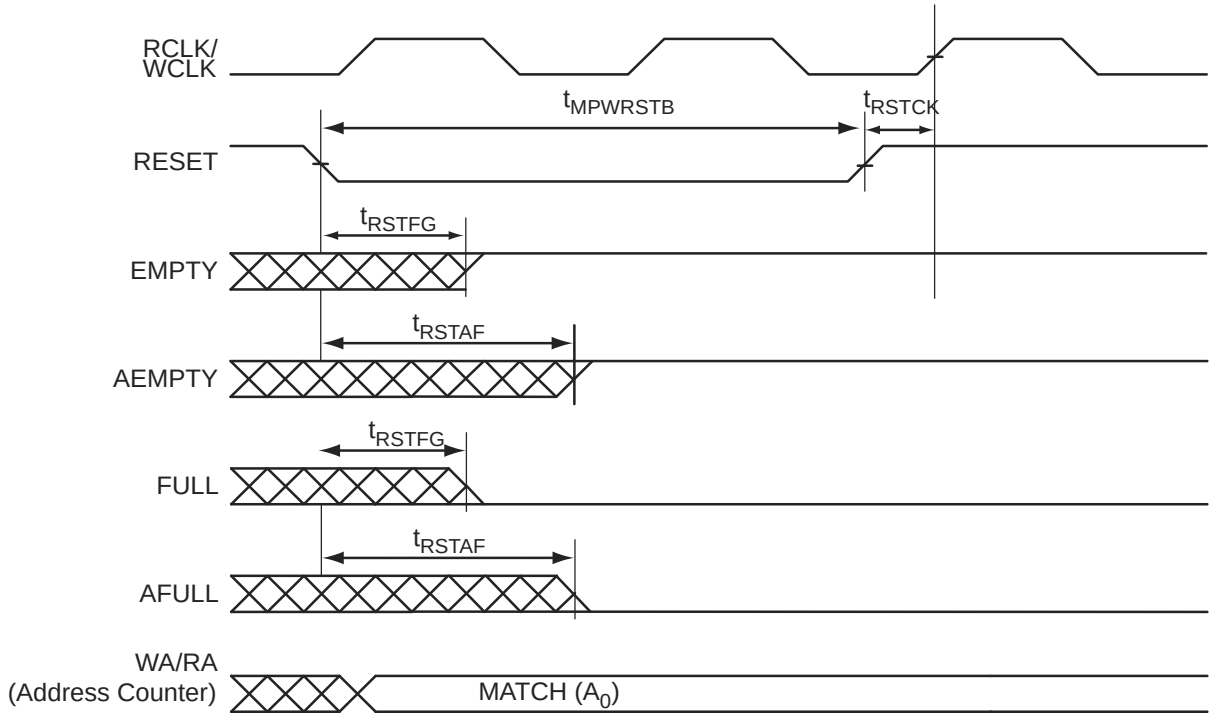


Figure 2-40 • **FIFO Reset**

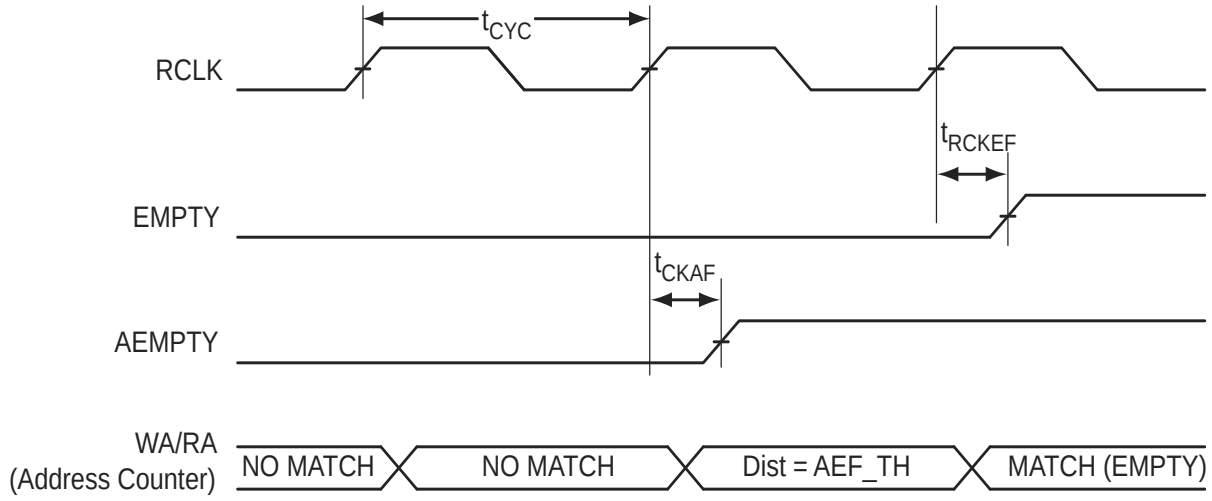


Figure 2-41 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

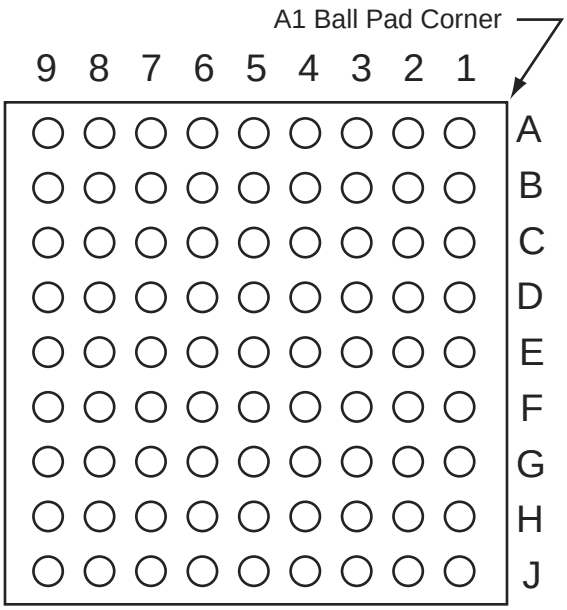
Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO a devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO FPGA Fabric User Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1* • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)**

IGLOO Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
CS281	W2
QN48	14
QN68	18
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

CS81



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS196	
Pin Number	**AGL125 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	**AGL125 Function**
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	**AGL125 Function**
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

CS196	
Pin Number	**AGL250 Function**
H11	GCB0/IO49NDB1
H12	GCA1/IO50PDB1
H13	IO51NDB1
H14	GCA2/IO51PDB1
J1	GFC2/IO105PDB3
J2	IO104PPB3
J3	IO106NPB3
J4	IO103PDB3
J5	IO103NDB3
J6	IO80RSB2
J7	VCC
J8	VCC
J9	IO64RSB2
J10	IO56PDB1
J11	GCB2/IO52PDB1
J12	IO52NDB1
J13	GDC1/IO58UDB1
J14	GDC0/IO58VDB1
K1	IO105NDB3
K2	GND
K3	IO104NPB3
K4	VCCIB3
K5	IO101PPB3
K6	IO91RSB2
K7	IO81RSB2
K8	IO73RSB2
K9	IO77RSB2
K10	IO56NDB1
K11	VCCIB1
K12	GDA1/IO60UPB1
K13	GND
K14	GDB1/IO59UDB1
L1	GEB1/IO99PDB3
L2	GEC1/IO100PDB3
L3	GEC0/IO100NDB3
L4	IO101NPB3

CS196	
Pin Number	**AGL250 Function**
L5	IO89RSB2
L6	IO92RSB2
L7	IO75RSB2
L8	IO66RSB2
L9	IO65RSB2
L10	IO71RSB2
L11	VPUMP
L12	VJTAG
L13	GDA0/IO60VPB1
L14	GDB0/IO59VDB1
M1	GEB0/IO99NDB3
M2	GEA1/IO98PPB3
M3	GNDQ
M4	VCCIB2
M5	IO88RSB2
M6	IO87RSB2
M7	IO82RSB2
M8	VCCIB2
M9	IO67RSB2
M10	GDB2/IO62RSB2
M11	VCCIB2
M12	VMV2
M13	TRST
M14	VCCIB1
N1	GEA0/IO98NPB3
N2	VMV3
N3	GEC2/IO95RSB2
N4	IO94RSB2
N5	GND
N6	IO86RSB2
N7	IO78RSB2
N8	IO74RSB2
N9	IO69RSB2
N10	GND
N11	TCK
N12	TDI

CS196	
Pin Number	**AGL250 Function**
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO97RSB2
P3	FF/GEB2/IO96RSB2
P4	IO90RSB2
P5	IO85RSB2
P6	IO83RSB2
P7	IO79RSB2
P8	IO76RSB2
P9	IO72RSB2
P10	IO68RSB2
P11	GDC2/IO63RSB2
P12	GDA2/IO61RSB2
P13	TMS
P14	GND

CS281	
Pin Number	AGL600 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO68NPB1
H16	GCB0/IO70NPB1
H18	GCA1/IO71PPB1
H19	GCA2/IO72PPB1
J1	VCOMPLF
J2	GFA0/IO162NDB3
J4	VCCPLF
J5	GFC0/IO164NPB3
J7	GFA2/IO161PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO69PPB1
J15	GCA0/IO71NPB1
J16	GCB2/IO73PPB1
J18	IO72NPB1
J19	IO75PSB1
K1	VCCIB3
K2	GFA1/IO162PDB3
K4	GND
K5	IO159NPB3
K7	IO161NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO74PPB1

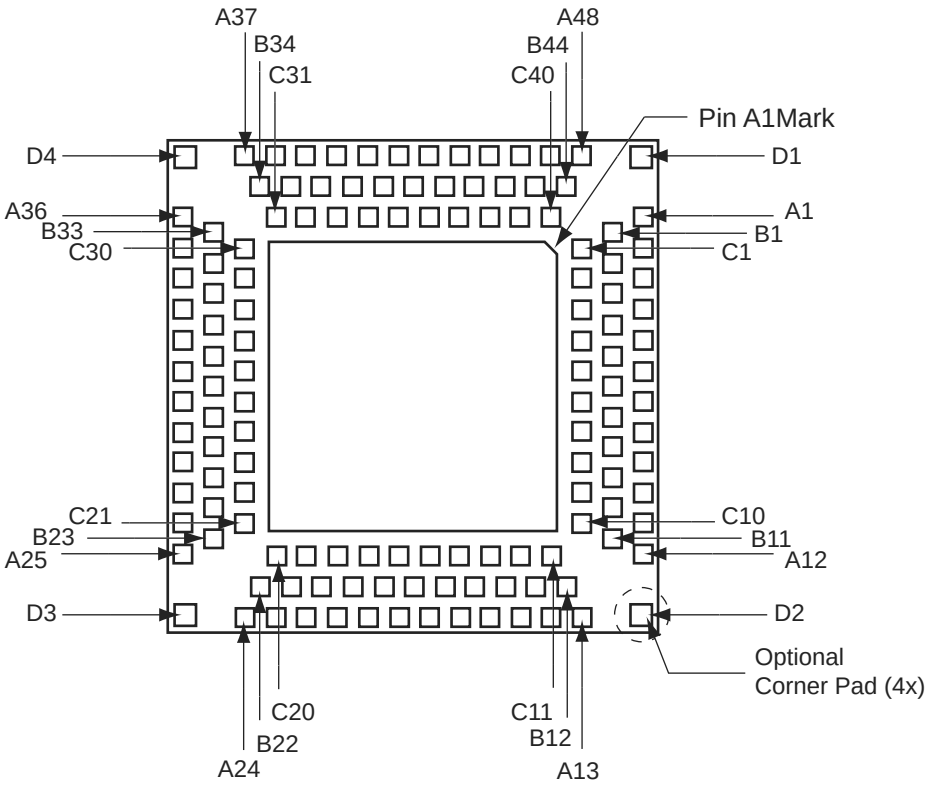
CS281	
Pin Number	AGL600 Function
K15	IO73NPB1
K16	GND
K18	IO74NPB1
K19	VCCIB1
L1	GFB2/IO160PDB3
L2	IO160NDB3
L4	GFC2/IO159PPB3
L5	IO153PPB3
L7	IO153NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO76PPB1
L15	IO76NPB1
L16	IO77PPB1
L18	IO78NPB1
L19	IO77NPB1
M1	IO158PDB3
M2	IO158NDB3
M4	IO154NPB3
M5	IO152PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO79NPB1
M16	IO81NPB1
M18	IO79PPB1
M19	IO78PPB1
N1	IO154PPB3
N2	IO152NPB3

CS281	
Pin Number	AGL600 Function
N4	IO150PPB3
N5	IO148NPB3
N7	GEA2/IO143RSB2
N8	VCCIB2
N9	IO117RSB2
N10	IO115RSB2
N11	IO114RSB2
N12	VCCIB2
N13	VPUMP
N15	IO82PPB1
N16	IO85PPB1
N18	IO82NPB1
N19	IO81PPB1
P1	IO151PDB3
P2	GND
P3	IO151NDB3
P4	IO149PPB3
P5	GEA0/IO144NPB3
P15	IO83NDB1
P16	IO83PDB1
P17	GDC1/IO86PPB1
P18	GND
P19	IO85NPB1
R1	IO150NPB3
R2	IO149NPB3
R4	GEC1/IO146PPB3
R5	GEB1/IO145PPB3
R6	IO138RSB2
R7	IO127RSB2
R8	IO123RSB2
R9	IO118RSB2
R10	IO111RSB2
R11	IO106RSB2
R12	IO103RSB2
R13	IO97RSB2
R14	IO95RSB2

CS281	
Pin Number	**AGL600 Function**
R15	IO94RSB2
R16	GDA1/IO88PPB1
R18	GDB0/IO87NPB1
R19	GDC0/IO86NPB1
T1	IO148PPB3
T2	GEC0/IO146NPB3
T4	GEB0/IO145NPB3
T5	IO132RSB2
T6	IO136RSB2
T7	IO130RSB2
T8	IO126RSB2
T9	IO120RSB2
T10	GND
T11	IO113RSB2
T12	IO104RSB2
T13	IO101RSB2
T14	IO98RSB2
T15	GDC2/IO91RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO87PPB1
U1	IO147PDB3
U2	GEA1/IO144PPB3
U6	IO131RSB2
U14	IO99RSB2
U18	TRST
U19	GDA0/IO88NPB1
V1	IO147NDB3
V2	VCCIB3
V3	GEC2/IO141RSB2
V4	IO140RSB2
V5	IO135RSB2
V6	GND
V7	IO125RSB2
V8	IO122RSB2
V9	IO116RSB2

CS281	
Pin Number	**AGL600 Function**
V10	IO112RSB2
V11	IO110RSB2
V12	IO108RSB2
V13	IO102RSB2
V14	GND
V15	IO93RSB2
V16	GDA2/IO89RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO142RSB2
W3	IO139RSB2
W4	IO137RSB2
W5	IO134RSB2
W6	IO133RSB2
W7	IO128RSB2
W8	IO124RSB2
W9	IO119RSB2
W10	VCCIB2
W11	IO109RSB2
W12	IO107RSB2
W13	IO105RSB2
W14	IO100RSB2
W15	IO96RSB2
W16	IO92RSB2
W17	GDB2/IO90RSB2
W18	TCK
W19	GND

QN132



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	**AGL400 Function**
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

Revision	Changes	Page
Revision 19	The following figures were deleted (SAR 29991). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 21770). Figure 2-36 • Write Access after Write onto Same Address Figure 2-37 • Read Access after Write onto Same Address Figure 2-38 • Write Access after Read onto Same Address The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-40 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SARs 29991, 30510).	N/A 2-119 to 2-130
	The "Pin Descriptions" chapter has been added (SAR 21642).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	4-1
	The "CS81" pin table for AGL250 is new (SAR 22737).	4-5
	The CS121 pin table for AGL125 is new (SAR 22737).	
	The P3 function was revised in the "CS196" pin table for AGL250 (SAR 24800).	4-12
	The "QN132" pin table for AGL250 was added. The "FG144" pin table for AGL060 was added (SAR 33689)	4-35, 4-42
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO Device Status" table indicates the status for each device in the device family.	N/A