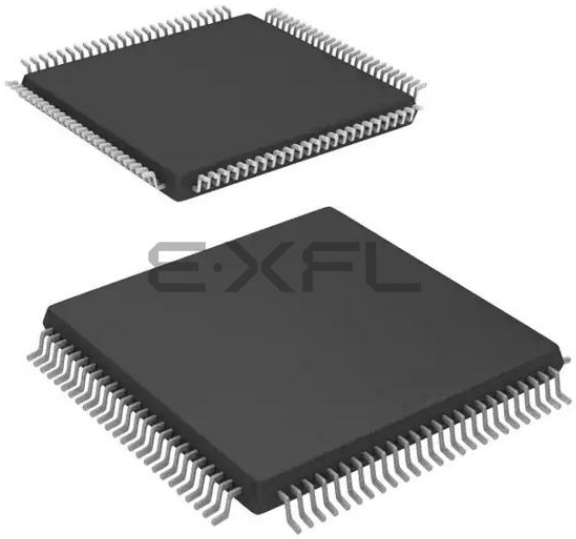

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6144 |
| Total RAM Bits | 36864 |
| Number of I/O | 68 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1agl250v2-vq100 |

## Flash*Freeze Technology

The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 12 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

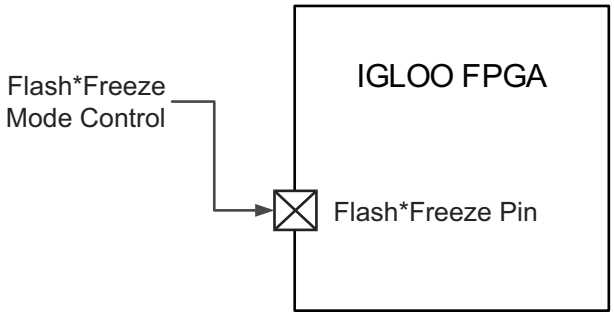



***Figure 1-3 •*** **IGLOO Flash*Freeze Mode**

## VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{PLUS®}$ core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

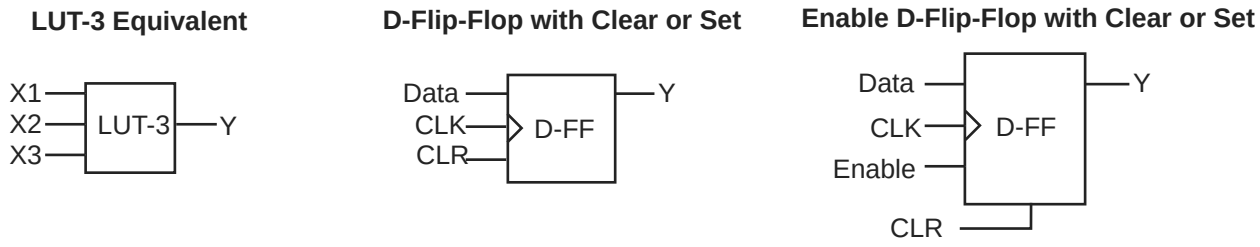



***Figure 1-4 •*** **VersaTile Configurations**

***Table 2-2 •*** **Recommended Operating Conditions** [1]

| Symbol | Parameter | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction Temperature [2] | | 0 to +85 | –40 to +100 | °C |
| VCC[3] | 1.5 V DC core supply voltage[5] | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.2 V–1.5 V wide range DC core supply voltage [4,6] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation [7] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL[8] | Analog power supply (PLL) | 1.5 V DC core supply voltage[5] | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | | 1.2 V – 1.5 V DC core supply voltage[4,6] | 1.14 to 1.575 | 1.14 to 1.575 | V |
| VCCI and VMV [9] | 1.2 V DC core supply voltage[6] | | 1.14 to 1.26 | 1.14 to 1.26 | V |
| | 1.2 V DC wide range DC supply voltage[6] | | 1.14 to 1.575 | 1.14 to 1.575 | V |
| | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.0 V DC supply voltage [10] | | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-24. VCCI should be at the same voltage within a given I/O bank.*
4. *All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.*
5. *For IGLOO® V5 devices*
6. *For IGLOO V2 devices only, operating at VCCI ≥ VCC.*
7. *VPUMP can be left floating during operation (not programming mode).*
8. *VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
9. *VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information.*
10. *3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.*

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

## PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC®3* and *ProASIC3E* FPGA fabric user guides for information on clock and lock recovery.

## Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

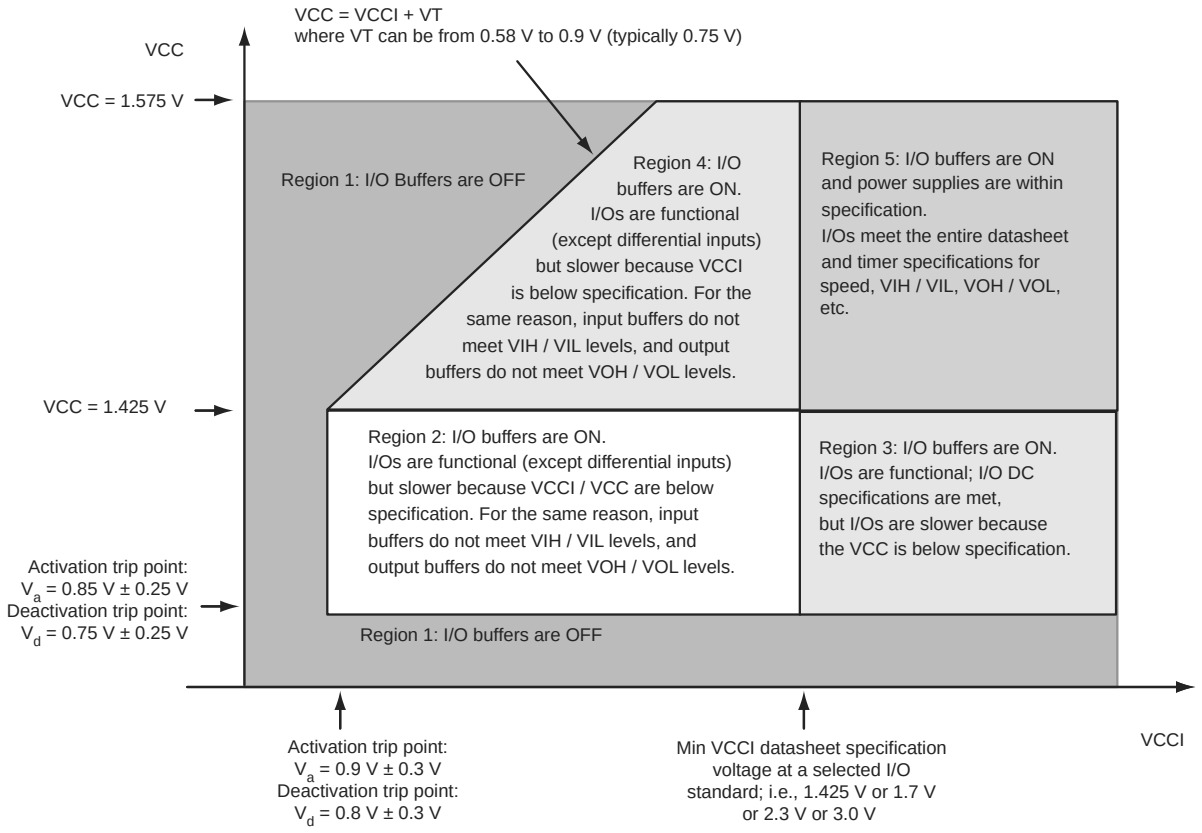



***Figure 2-1 •*** **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

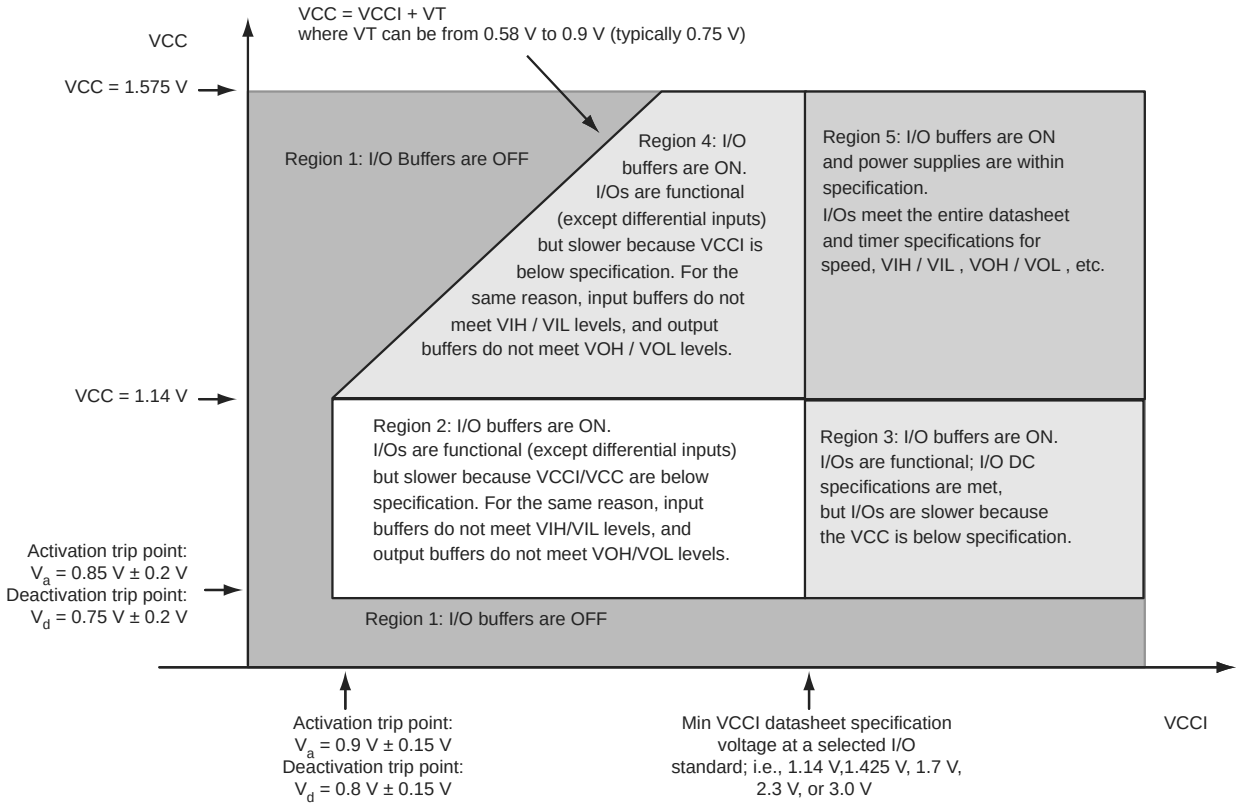



***Figure 2-2 •*** **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

# Thermal Characteristics

## *Introduction*

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

*EQ 1*

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

## Power per I/O Pin

***Table 2-13 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks**

| | VCCI (V) | Static Power PDC6 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | – | 16.27 |
| 3.3 V LVCMOS Wide Range[3] | 3.3 | – | 16.27 |
| 2.5 V LVCMOS | 2.5 | – | 4.65 |
| 1.8 V LVCMOS | 1.8 | – | 1.61 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 0.96 |
| 1.2 V LVCMOS[4] | 1.2 | – | 0.58 |
| 1.2 V LVCMOS Wide Range[4] | 1.2 | – | 0.58 |
| 3.3 V PCI | 3.3 | – | 17.67 |
| 3.3 V PCI-X | 3.3 | – | 17.67 |
| **Differential** | | | |
| LVDS | 2.5 | 2.26 | 23.39 |
| LVPECL | 3.3 | 5.72 | 59.05 |

*Notes:*

1. *$P_{DC6}$ is the static power (where applicable) measured on VCCI.*
2. *$P_{AC9}$ is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO V2 devices only*

***Table 2-14 •*** **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

| | VCCI (V) | Static Power PDC6 (mW)[1] | Dynamic Power PAC9 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | – | 16.41 |
| 3.3 V LVCMOS Wide Range[3] | 3.3 | – | 16.41 |
| 2.5 V LVCMOS | 2.5 | – | 4.75 |
| 1.8 V LVCMOS | 1.8 | – | 1.66 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | – | 1.00 |
| 1.2 V LVCMOS[4] | 1.2 | – | 0.61 |
| 1.2 V LVCMOS Wide Range[4] | 1.2 | – | 0.61 |
| 3.3 V PCI | 3.3 | – | 17.78 |
| 3.3 V PCI-X | 3.3 | – | 17.78 |

*Notes:*

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *Applicable for IGLOO V2 devices only.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

# User I/O Characteristics

## Timing Model

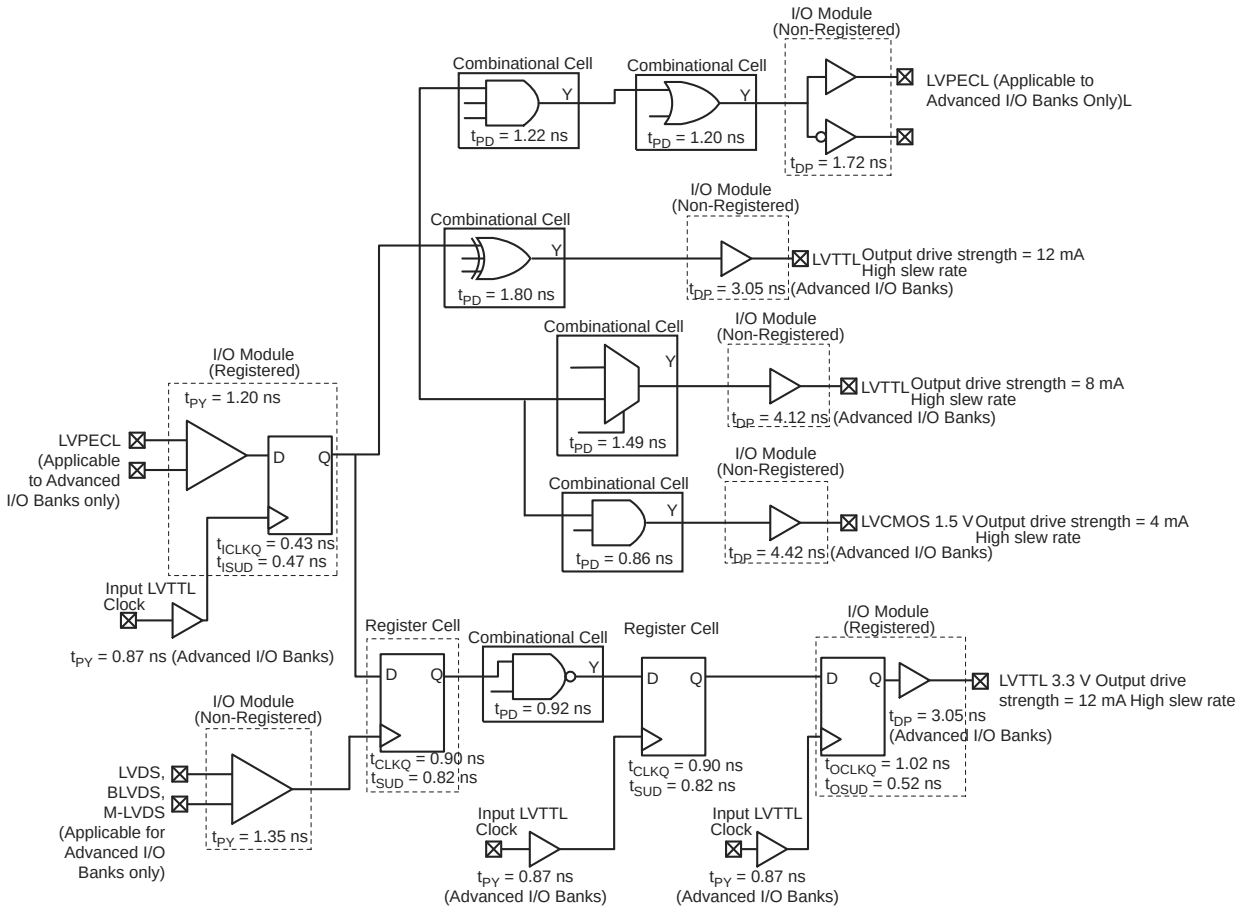



***Figure 2-3 •*** **Timing Model**
**Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices**

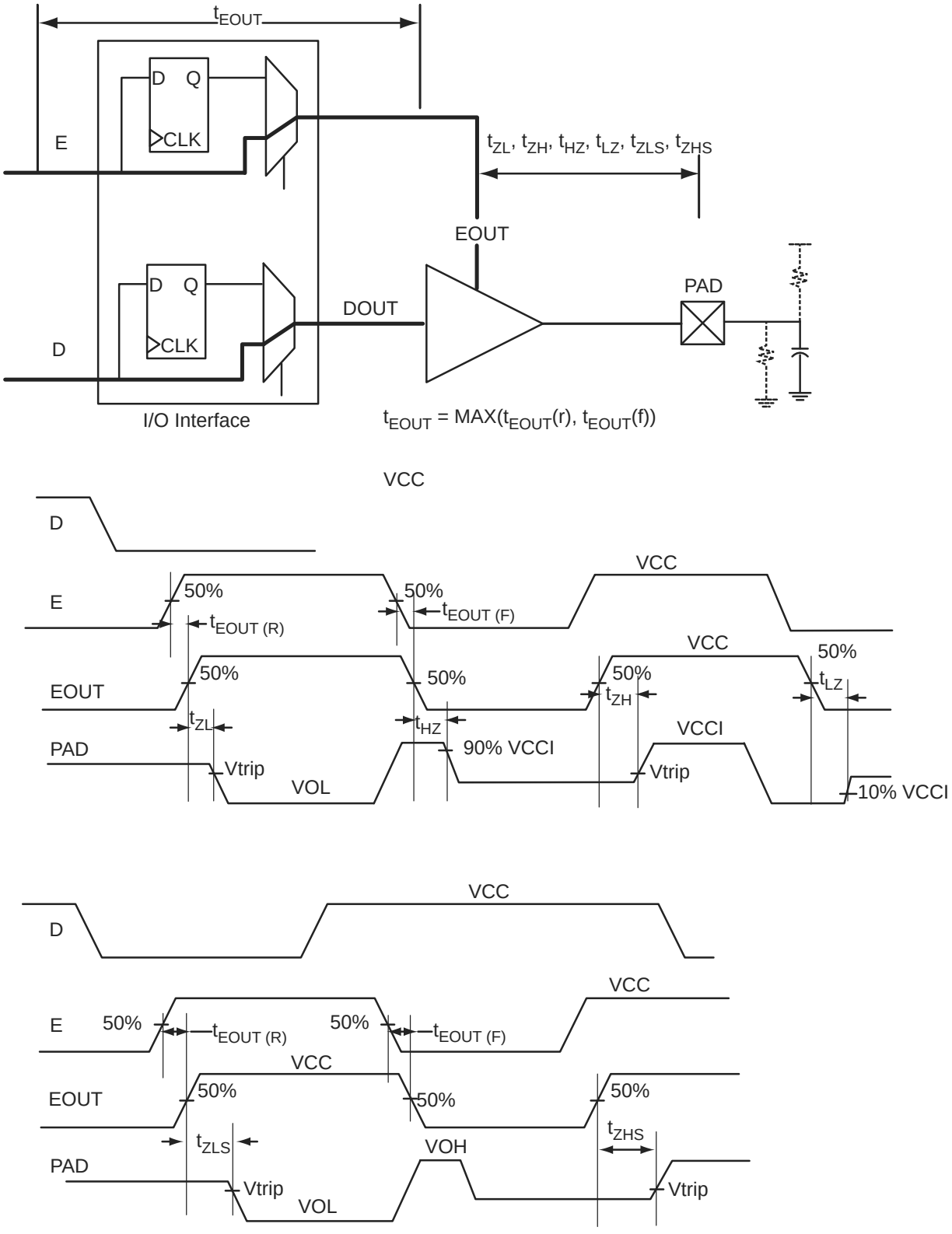



***Figure 2-6 •*** **Tristate Output Buffer Timing Model and Delays (example)**

***Table 2-28 •*** **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

| | Commercial[1] | | Industrial[2] | |
|---|---|---|---|---|
| | IIL[4] | IIH[5] | IIL[4] | IIH[5] |
| **DC I/O Standards** | **µA** | **µA** | **µA** | **µA** |
| 3.3 V LVTTL / 3.3 V LVCMOS | 10 | 10 | 15 | 15 |
| 3.3 V LVCMOS Wide Range | 10 | 10 | 15 | 15 |
| 2.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.8 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.5 V LVCMOS | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS[3] | 10 | 10 | 15 | 15 |
| 1.2 V LVCMOS Wide Range[3] | 10 | 10 | 15 | 15 |
| 3.3 V PCI | 10 | 10 | 15 | 15 |
| 3.3 V PCI-X | 10 | 10 | 15 | 15 |

*Notes:*

1. *Commercial range (0°C < $T_A$ < 70°C)*
2. *Industrial range (–40°C < $T_A$ < 85°C)*
3. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
5. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

***Table 2-34 •*** **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | 5 | – | 1.55 | 2.67 | 0.26 | 0.98 | 1.10 | 2.71 | 2.18 | 3.25 | 3.93 | 8.50 | 7.97 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 5 | – | 1.55 | 3.73 | 0.26 | 1.32 | 1.10 | 3.73 | 2.91 | 4.51 | 5.43 | 9.52 | 8.69 | ns |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | 5 | – | 1.55 | 2.64 | 0.26 | 1.20 | 1.10 | 2.67 | 2.29 | 3.30 | 3.79 | 8.46 | 8.08 | ns |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | 5 | – | 1.55 | 2.72 | 0.26 | 1.11 | 1.10 | 2.76 | 2.43 | 3.58 | 4.19 | 8.55 | 8.22 | ns |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | 5 | – | 1.55 | 2.96 | 0.26 | 1.27 | 1.10 | 3.00 | 2.70 | 3.75 | 4.23 | 8.78 | 8.48 | ns |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | 5 | – | 1.55 | 3.60 | 0.26 | 1.60 | 1.10 | 3.47 | 3.36 | 3.93 | 3.65 | 9.26 | 9.14 | ns |
| 1.2 V LVCMOS Wide Range[3] | 100 µA | 2 mA | High | 5 | – | 1.55 | 3.60 | 0.26 | 1.60 | 1.10 | 3.47 | 3.36 | 3.93 | 3.65 | 9.26 | 9.14 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25[2] | 1.55 | 2.91 | 0.26 | 0.86 | 1.10 | 2.95 | 2.29 | 3.25 | 3.93 | 8.74 | 8.08 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25[2] | 1.55 | 2.91 | 0.25 | 0.86 | 1.10 | 2.95 | 2.29 | 3.25 | 3.93 | 8.74 | 8.08 | ns |
| LVDS | 24 mA | – | High | – | – | 1.55 | 2.27 | 0.25 | 1.57 | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | – | High | – | – | 1.55 | 2.24 | 0.25 | 1.38 | – | – | – | – | – | – | – | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-147 •*** **Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL[1] | Output Lower Current | 0.65 | 0.91 | 1.16 | mA |
| IOH[1] | Output High Current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIH[2] | Input High Leakage Current | | | 10 | µA |
| IIL[2] | Input Low Leakage Current | | | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common-Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common-Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF[4] | Input Differential Voltage | 100 | 350 | | mV |

*Notes:*

1. *IOL/IOH is defined by VODIFF/(resistor network)*
2. *Currents are measured at 85°C junction temperature.*

***Table 2-148 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---|---|---|
| 1.075 | 1.325 | Cross point |

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-149 •*** **LVDS – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.97 | 1.67 | 0.19 | 1.31 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.*

#### *1.2 V DC Core Voltage*

***Table 2-150 •*** **LVDS – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 1.55 | 2.19 | 0.25 | 1.52 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.*

## I/O Register Specifications

### *Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset*

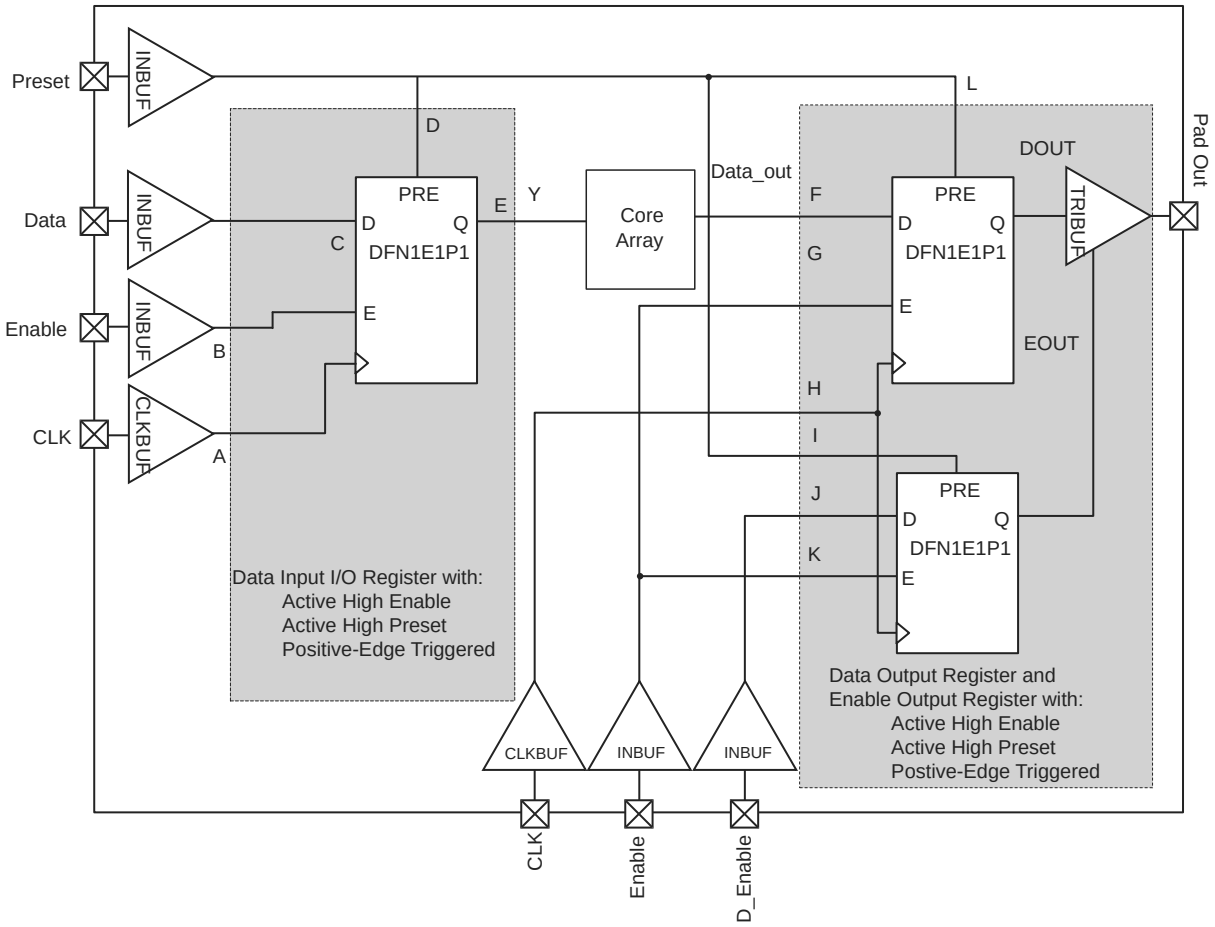



***Figure 2-16 •*** **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

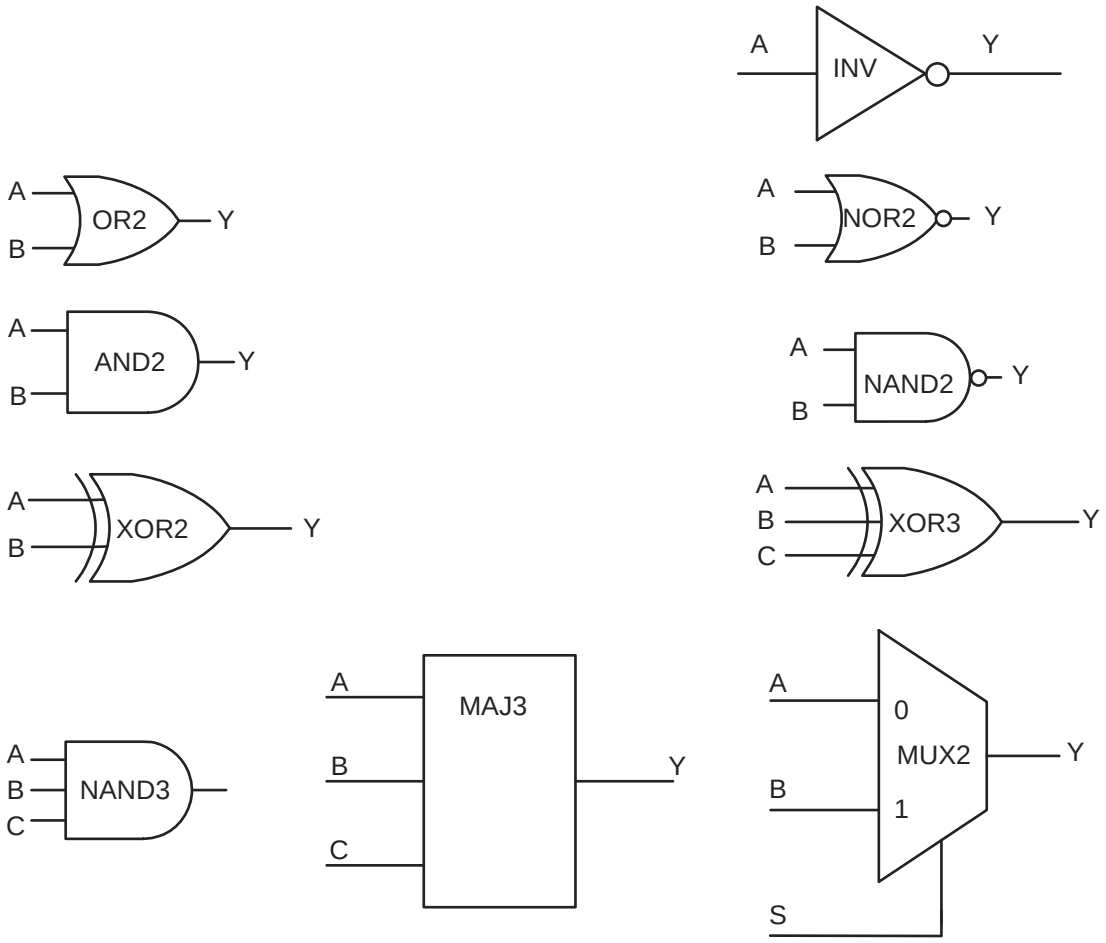



***Figure 2-25 •*** **Sample of Combinatorial Cells**

## VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

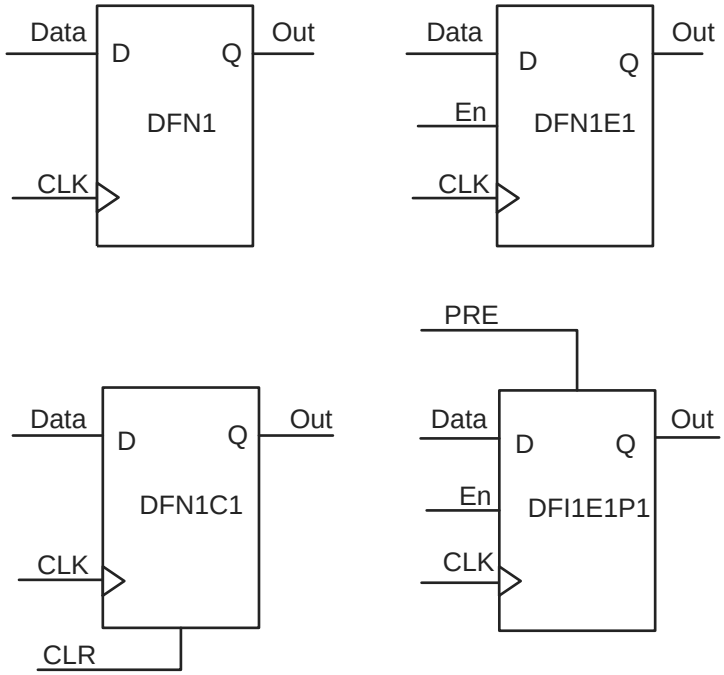



***Figure 2-27 •*** **Sample of Sequential Cells**

***Table 2-179 •*** **AGL600 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.48 | 1.82 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.52 | 1.94 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-180 •*** **AGL1000 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.55 | 1.89 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.60 | 2.02 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.15 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.42 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

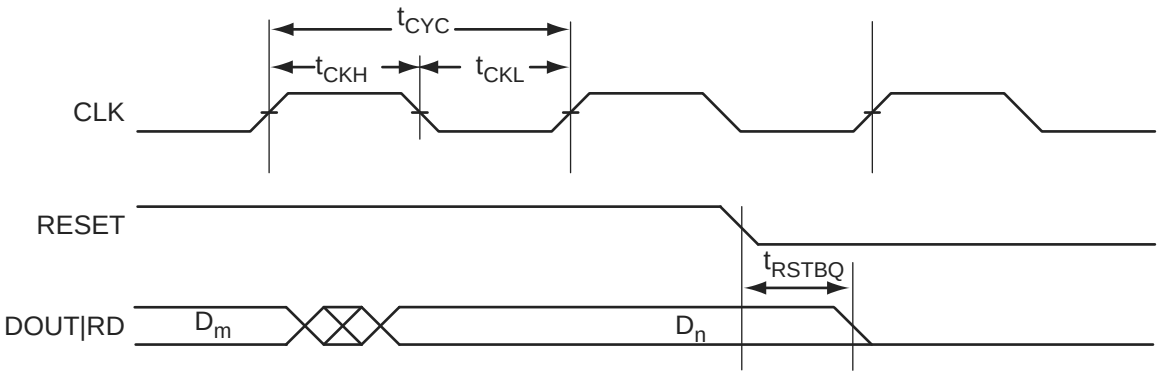



***Figure 2-36 •*** **RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-195 • FIFO**

**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

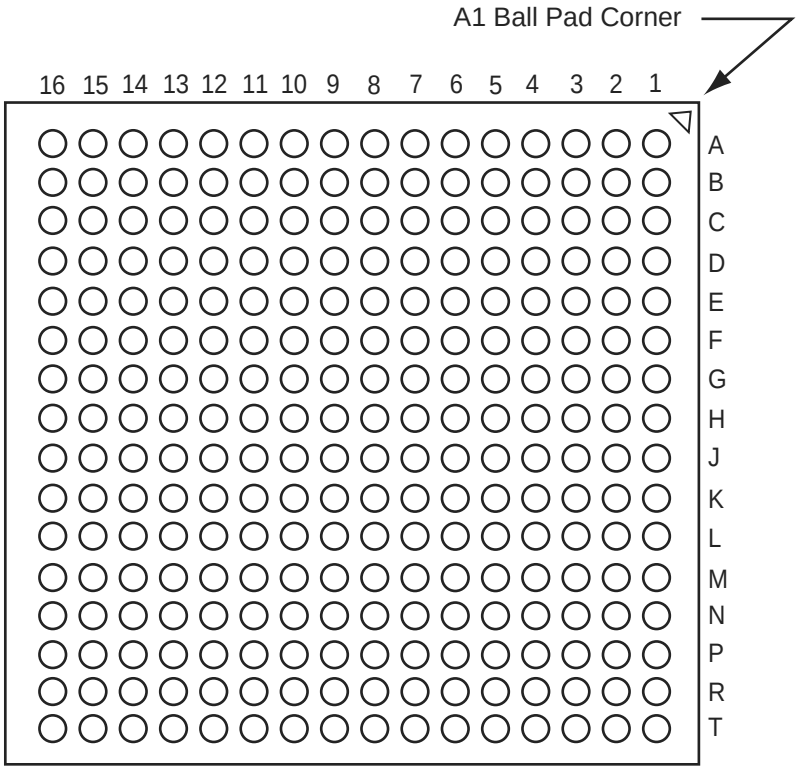
| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.99 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.16 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.30 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.76 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.25 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 3.33 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 1.80 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 3.53 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 3.35 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 12.85 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 3.48 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 12.72 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 2.02 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 2.02 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.68 | ns |
| $t_{CYC}$ | Clock Cycle Time | 6.24 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 160 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

| QN68 | |
|---|---|
| **Pin Number** | **AGL030 Function** |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | FF/IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |
| 36 | TDO |

| QN68 | |
|---|---|
| **Pin Number** | **AGL030 Function** |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | VCCIB0 |
| 60 | GND |
| 61 | VCC |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

# FG256

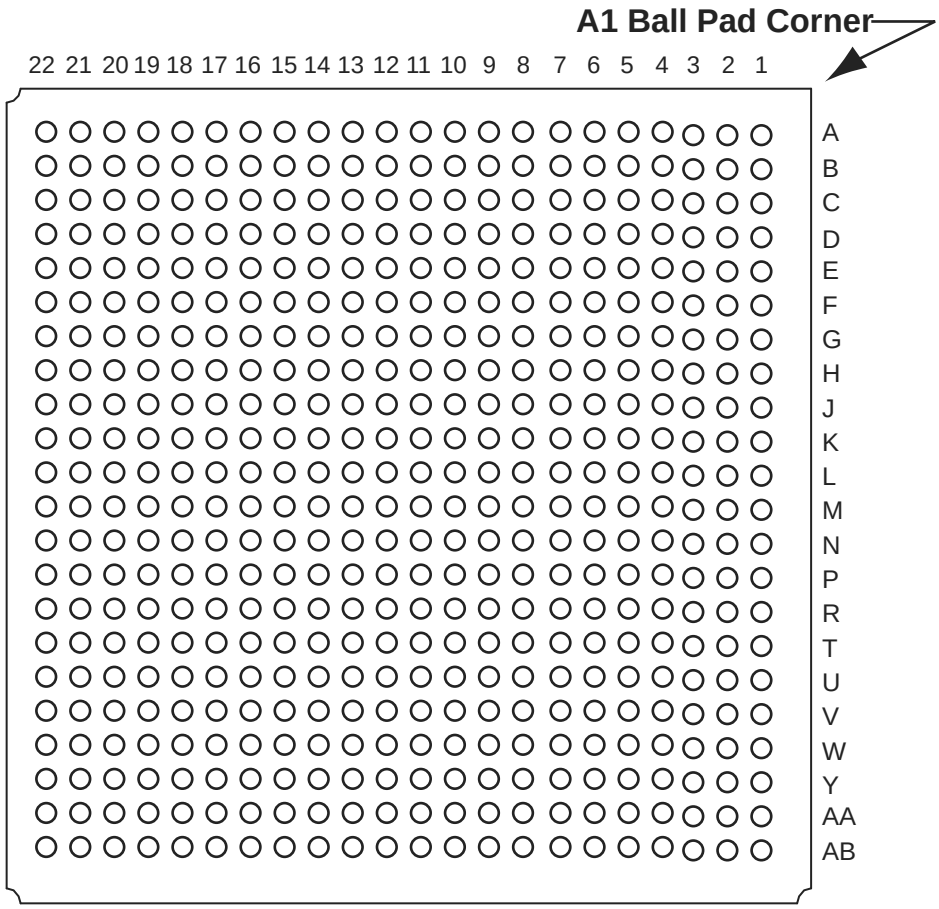



*Note: This is the bottom view of the package.*

## Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

# FG484




*Note: This is the bottom view of the package.*

## Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| N17 | IO80NPB1 |
| N18 | IO74NPB1 |
| N19 | IO72NDB1 |
| N20 | NC |
| N21 | IO79NPB1 |
| N22 | NC |
| P1 | NC |
| P2 | IO153PDB3 |
| P3 | IO153NDB3 |
| P4 | IO159NDB3 |
| P5 | IO156NPB3 |
| P6 | IO151PPB3 |
| P7 | IO158PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO87NPB1 |
| P17 | IO85NDB1 |
| P18 | IO85PDB1 |
| P19 | IO84PDB1 |
| P20 | NC |
| P21 | IO81PDB1 |
| P22 | NC |
| R1 | NC |
| R2 | NC |
| R3 | VCC |
| R4 | IO150PDB3 |
| R5 | IO151NPB3 |
| R6 | IO147NPB3 |
| R7 | GEC0/IO146NPB3 |
| R8 | VMV3 |