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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	68
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl250v2-vq100i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.



Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)



Figure 1-2 • IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T <sub>STG</sub> (°C) <sup>2</sup>	Maximum Operating Junction Temperature T <sub>J</sub> (°C) <sup>2</sup>
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature<sup>1</sup>

Notes:

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 on page 2-2 for device operating conditions and absolute limits.

#### Table 2-4 • Overshoot and Undershoot Limits<sup>1</sup>

vcci	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle <sup>2</sup>	Maximum Overshoot/ Undershoot <sup>2</sup>
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at junction temperature at 85°C.

2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

3. This table does not provide PCI overshoot/undershoot limits.

# I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

- 1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
- 2. VCCI > VCC 0.75 V (typical)
- 3. Chip is in the operating mode.

#### VCCI Trip Point:

Ramping up (V5 devices): 0.6 V < trip\_point\_up < 1.2 V Ramping down (V5 Devices): 0.5 V < trip\_point\_down < 1.1 V Ramping up (V2 devices): 0.75 V < trip\_point\_up < 1.05 V Ramping down (V2 devices): 0.65 V < trip\_point\_down < 0.95 V

#### VCC Trip Point:

Ramping up (V5 devices): 0.6 V < trip\_point\_up < 1.1 V Ramping down (V5 devices): 0.5 V < trip\_point\_down < 1.0 V

### Summary of I/O Timing Characteristics – Default I/O Software Settings

#### Table 2-29 • Summary of AC Measuring Points

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
3.3 V VCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

#### Table 2-30 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t <sub>DP</sub>	Data to Pad delay through the Output Buffer
t <sub>PY</sub>	Pad to Data delay through the Input Buffer
t <sub>DOUT</sub>	Data to Output Buffer delay through the I/O interface
t <sub>EOUT</sub>	Enable to Output Buffer Tristate Control delay through the I/O interface
t <sub>DIN</sub>	Input Buffer to Data delay through the I/O interface
t <sub>HZ</sub>	Enable to Pad delay through the Output Buffer—High to Z
t <sub>ZH</sub>	Enable to Pad delay through the Output Buffer—Z to High
t <sub>LZ</sub>	Enable to Pad delay through the Output Buffer—Low to Z
t <sub>ZL</sub>	Enable to Pad delay through the Output Buffer—Z to Low
t <sub>ZHS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t <sub>ZLS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

#### Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage<br/>Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V<br/>Applicable to Standard Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

#### Table 2-56 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

#### Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

#### **Timing Characteristics**

Applies to 1.5 V DC Core Voltage

# Table 2-67 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage<br/>Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V<br/>Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>dout</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 µA	2 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	4 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	6 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	8 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	12 mA	Std.	0.97	4.69	0.18	1.19	0.66	4.71	4.25	3.80	4.10	8.31	7.85	ns
100 µA	16 mA	Std.	0.97	4.46	0.18	1.19	0.66	4.48	4.11	3.86	4.21	8.07	7.71	ns
100 µA	24 mA	Std.	0.97	4.34	0.18	1.19	0.66	4.36	4.14	3.93	4.64	7.95	7.74	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 μA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

 Table 2-68 •
 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage

 Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

 Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>eout</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 µA	2 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	4 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	6 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	8 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	12 mA	Std.	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
100 µA	16 mA	Std.	0.97	2.87	0.18	1.19	0.66	2.89	2.22	3.86	4.41	6.49	5.82	ns
100 µA	24 mA	Std.	0.97	2.90	0.18	1.19	0.66	2.92	2.16	3.94	4.86	6.51	5.75	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

2. Software default selection highlighted in gray.

3. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 μA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

#### 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	VIL		ИН		VOL	VОН	IOL	юн	IOSH	IOSL	IIL¹	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

## Table 2-79 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

 Table 2-80 •
 Minimum and Maximum DC Input and Output Levels

 Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	vон	IOL	юн	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

#### Table 2-135 • 1.2 V LVCMOS High Slew

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Commercial-Case Conditions: T_J = 70^{\circ}C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Banks
```

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	Std.	1.55	8.57	0.26	1.53	1.10	8.23	7.38	2.51	2.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

# Table 2-136 • 1.2 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

#### **Applicable to Standard Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	Std.	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

#### 1.2 V LVCMOS Wide Range

#### Table 2-137 • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Advanced I/O Banks

1.2 V LVCI Wide Rang	MOS ge		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 µA	2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 μA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

- 3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
- 4. Currents are measured at 100°C junction temperature and maximum voltage.
- 5. Currents are measured at 85°C junction temperature.
- 6. Software default selection highlighted in gray.

#### Table 2-177 • AGL250 Global Resource

Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V

		Std.		
Parameter	Description	Min. <sup>1</sup> Max. <sup>2</sup>		Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	1.39	1.73	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	1.41	1.84	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock	1.18		ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock	1.15		ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

#### Table 2-178 • AGL400 Global Resource

#### Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V

		Std.		
Parameter	rameter Description		Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	1.45	1.79	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	1.48	1.91	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock	1.18		ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock	1.15		ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-7 for derating values.

## **Clock Conditioning Circuits**

#### **CCC Electrical Specifications**

#### **Timing Characteristics**

#### Table 2-189 • IGLOO CCC/PLL Specification

For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Тур.	Max.	Units
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f <sub>OUT_CCC</sub>	0.75		250	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		360 <sup>3</sup>		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL <sup>4, 5</sup>			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter <sup>6</sup>				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1, 2</sup>	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2</sup>	0.469		15.65	ns
Delay Range in Block: Fixed Delay <sup>1, 2</sup>		3.5		ns
CCC Output Peak-to-Peak Period Jitter F <sub>CCC_OUT</sub>	Maxim	um Peak-to-	Peak Jitter Da	ta <sup>7</sup>
	$SSO \geq 4^8$	$SSO \geq 8^8$	$SSO \ge 16^8$	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.

2.  $T_J = 25^{\circ}C, V_{CC} = 1.5 V$ 

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4. The AGL030 device does not support a PLL.

5. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

7. Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.

8. Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.

#### *Table 2-194* • RAM512X18

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t <sub>AS</sub>	Address setup time	1.53	ns
t <sub>AH</sub>	Address hold time	0.29	ns
t <sub>ENS</sub>	REN, WEN setup time	1.36	ns
t <sub>ENH</sub>	REN, WEN hold time	0.15	ns
t <sub>DS</sub>	Input data (WD) setup time	1.33	ns
t <sub>DH</sub>	Input data (WD) hold time	0.66	ns
t <sub>CKQ1</sub>	Clock High to new data valid on RD (output retained)	7.88	ns
t <sub>CKQ2</sub>	Clock High to new data valid on RD (pipelined)	3.20	ns
t <sub>C2CRWH</sub> 1	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.87	ns
t <sub>C2CWRH</sub> 1	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.04	ns
t <sub>RSTBQ</sub>	RESET Low to data out Low on RD (flow through)	3.86	ns
	RESET Low to data out Low on RD (pipelined)	3.86	ns
t <sub>REMRSTB</sub>	RESET removal	1.12	ns
t <sub>RECRSTB</sub>	RESET recovery	5.93	ns
t <sub>MPWRSTB</sub>	RESET minimum pulse width	1.18	ns
t <sub>CYC</sub>	Clock cycle time	10.90	ns
F <sub>MAX</sub>	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

### **Embedded FlashROM Characteristics**



Figure 2-45 • Timing Diagram

#### **Timing Characteristics**

1.5 V DC Core Voltage

# Table 2-197 • Embedded FlashROM Access TimeWorst Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t <sub>SU</sub>	Address Setup Time	0.57	ns
t <sub>HOLD</sub>	Address Hold Time	0.00	ns
t <sub>СК2Q</sub>	Clock to Out	34.14	ns
F <sub>MAX</sub>	Maximum Clock Frequency	15	MHz

#### 1.2 V DC Core Voltage

# Table 2-198 • Embedded FlashROM Access TimeWorst Commercial-Case Conditions: $T_J = 70^{\circ}$ C, VCC = 1.14 V

Parameter	Description	Std.	Units
t <sub>SU</sub>	Address Setup Time	0.59	ns
t <sub>HOLD</sub>	Address Hold Time	0.00	ns
t <sub>CK2Q</sub>	Clock to Out	52.90	ns
F <sub>MAX</sub>	Maximum Clock Frequency	10	MHz

# 3 – Pin Descriptions

### **Supply Pins**

#### GND

#### Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

#### GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

#### VCC

#### **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices, and 1.2 V or 1.5 V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

#### VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

#### VMVx I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

#### VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

- 1.5 V for IGLOO V5 devices
- 1.2 V or 1.5 V for IGLOO V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

• There is one VCCPLF pin on IGLOO devices.

#### VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-androute tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.



Package Pin Assignments

	CS121
Pin Number	AGL060 Function
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1





Note: This is the bottom view of the package.

#### Note

For more information on package drawings, see PD3068: Package Mechanical Drawings.

### Microsemi

IGLOO Low Power Flash FPGAs

	FG144		FG144		FG144
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
A1	GNDQ	D1	IO128RSB1	G1	GFA1/IO121RSB1
A2	VMV0	D2	IO129RSB1	G2	GND
A3	GAB0/IO02RSB0	D3	IO130RSB1	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO67RSB1	G4	GFA0/IO122RSB1
A5	IO11RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO18RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO61RSB0
A9	IO25RSB0	D9	GBB2/IO43RSB0	G9	IO48RSB0
A10	GBA0/IO39RSB0	D10	IO28RSB0	G10	GCC2/IO59RSB0
A11	GBA1/IO40RSB0	D11	IO44RSB0	G11	IO47RSB0
A12	GNDQ	D12	GCB1/IO53RSB0	G12	GCB2/IO58RSB0
B1	GAB2/IO69RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO125RSB1	H2	GFB2/IO119RSB1
B3	GAA0/IO00RSB0	E3	GFC1/IO126RSB1	H3	GFC2/IO118RSB1
B4	GAA1/IO01RSB0	E4	VCCIB1	H4	GEC1/IO112RSB1
B5	IO08RSB0	E5	IO68RSB1	H5	VCC
B6	IO14RSB0	E6	VCCIB0	H6	IO50RSB0
B7	IO19RSB0	E7	VCCIB0	H7	IO60RSB0
B8	IO22RSB0	E8	GCC1/IO51RSB0	H8	GDB2/IO71RSB1
B9	GBB0/IO37RSB0	E9	VCCIB0	H9	GDC0/IO62RSB0
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO56RSB0	H11	IO49RSB0
B12	VMV0	E12	IO46RSB0	H12	VCC
C1	IO132RSB1	F1	GFB0/IO123RSB1	J1	GEB1/IO110RSB1
C2	GFA2/IO120RSB1	F2	VCOMPLF	J2	IO115RSB1
C3	GAC2/IO131RSB1	F3	GFB1/IO124RSB1	J3	VCCIB1
C4	VCC	F4	IO127RSB1	J4	GEC0/IO111RSB1
C5	IO10RSB0	F5	GND	J5	IO116RSB1
C6	IO12RSB0	F6	GND	J6	IO117RSB1
C7	IO21RSB0	F7	GND	J7	VCC
C8	IO24RSB0	F8	GCC0/IO52RSB0	J8	TCK
C9	IO27RSB0	F9	GCB0/IO54RSB0	J9	GDA2/IO70RSB1
C10	GBA2/IO41RSB0	F10	GND	J10	TDO
C11	IO42RSB0	F11	GCA1/IO55RSB0	J11	GDA1/IO65RSB0
C12	GBC2/IO45RSB0	F12	GCA2/IO57RSB0	J12	GDB1/IO63RSB0

### Microsemi

Package Pin Assignments

FG256			FG256		FG256		
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function		
H3	GFB1/IO163PPB3	K9	GND	M15	GDC1/IO86PDB1		
H4	VCOMPLF	K10	GND	M16	IO84NDB1		
H5	GFC0/IO164NPB3	K11	VCC	N1	IO150NDB3		
H6	VCC	K12	VCCIB1	N2	IO147PPB3		
H7	GND	K13	IO73NPB1	N3	GEC1/IO146PPB3		
H8	GND	K14	IO80NPB1	N4	IO140RSB2		
H9	GND	K15	IO74NPB1	N5	GNDQ		
H10	GND	K16	IO72NDB1	N6	GEA2/IO143RSB2		
H11	VCC	L1	IO159NDB3	N7	IO126RSB2		
H12	GCC0/IO69NPB1	L2	IO156NPB3	N8	IO120RSB2		
H13	GCB1/IO70PPB1	L3	IO151PPB3	N9	IO108RSB2		
H14	GCA0/IO71NPB1	L4	IO158PSB3	N10	IO103RSB2		
H15	IO67NPB1	L5	VCCIB3	N11	IO99RSB2		
H16	GCB0/IO70NPB1	L6	GND	N12	GNDQ		
J1	GFA2/IO161PPB3	L7	VCC	N13	IO92RSB2		
J2	GFA1/IO162PDB3	L8	VCC	N14	VJTAG		
J3	VCCPLF	L9	VCC	N15	GDC0/IO86NDB1		
J4	IO160NDB3	L10	VCC	N16	GDA1/IO88PDB1		
J5	GFB2/IO160PDB3	L11	GND	P1	GEB1/IO145PDB3		
J6	VCC	L12	VCCIB1	P2	GEB0/IO145NDB3		
J7	GND	L13	GDB0/IO87NPB1	P3	VMV2		
J8	GND	L14	IO85NDB1	P4	IO138RSB2		
J9	GND	L15	IO85PDB1	P5	IO136RSB2		
J10	GND	L16	IO84PDB1	P6	IO131RSB2		
J11	VCC	M1	IO150PDB3	P7	IO124RSB2		
J12	GCB2/IO73PPB1	M2	IO151NPB3	P8	IO119RSB2		
J13	GCA1/IO71PPB1	M3	IO147NPB3	P9	IO107RSB2		
J14	GCC2/IO74PPB1	M4	GEC0/IO146NPB3	P10	IO104RSB2		
J15	IO80PPB1	M5	VMV3	P11	IO97RSB2		
J16	GCA2/IO72PDB1	M6	VCCIB2	P12	VMV1		
K1	GFC2/IO159PDB3	M7	VCCIB2	P13	TCK		
K2	IO161NPB3	M8	IO117RSB2	P14	VPUMP		
K3	IO156PPB3	M9	IO110RSB2	P15	TRST		
K4	IO129RSB2	M10	VCCIB2	P16	GDA0/IO88NDB1		
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO144PDB3		
K6	VCC	M12	VMV2	R2	GEA0/IO144NDB3		
K7	GND	M13	IO94RSB2	R3	IO139RSB2		
K8	GND	M14	GDB1/IO87PPB1	R4	GEC2/IO141RSB2		



	FG484
Pin Number	AGL400 Function
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

FG484		
Pin Number	AGL600 Function	
C21	NC	
C22	VCCIB1	
D1	NC	
D2	NC	
D3	NC	
D4	GND	
D5	GAA0/IO00RSB0	
D6	GAA1/IO01RSB0	
D7	GAB0/IO02RSB0	
D8	IO11RSB0	
D9	IO16RSB0	
D10	IO18RSB0	
D11	IO28RSB0	
D12	IO34RSB0	
D13	IO37RSB0	
D14	IO41RSB0	
D15	IO43RSB0	
D16	GBB1/IO57RSB0	
D17	GBA0/IO58RSB0	
D18	GBA1/IO59RSB0	
D19	GND	
D20	NC	
D21	NC	
D22	NC	
E1	NC	
E2	NC	
E3	GND	
E4	GAB2/IO173PDB3	
E5	GAA2/IO174PDB3	
E6	GNDQ	
E7	GAB1/IO03RSB0	
E8	IO13RSB0	
E9	IO14RSB0	
E10	IO21RSB0	
E11	IO27RSB0	
E12	IO32RSB0	

FG484		
Pin Number	AGL1000 Function	
AA15	NC	
AA16	IO122RSB2	
AA17	IO119RSB2	
AA18	IO117RSB2	
AA19	NC	
AA20	NC	
AA21	VCCIB1	
AA22	GND	
AB1	GND	
AB2	GND	
AB3	VCCIB2	
AB4	IO180RSB2	
AB5	IO176RSB2	
AB6	IO173RSB2	
AB7	IO167RSB2	
AB8	IO162RSB2	
AB9	IO156RSB2	
AB10	IO150RSB2	
AB11	IO145RSB2	
AB12	IO144RSB2	
AB13	IO132RSB2	
AB14	IO127RSB2	
AB15	IO126RSB2	
AB16	IO123RSB2	
AB17	IO121RSB2	
AB18	IO118RSB2	
AB19	NC	
AB20	VCCIB2	
AB21	GND	
AB22	GND	
B1	GND	
B2	VCCIB3	
B3	NC	
B4	IO06RSB0	
B5	IO08RSB0	
B6	IO12RSB0	

FG484		
Pin Number	AGL1000 Function	
N17	IO100NPB1	
N18	IO102NDB1	
N19	IO102PDB1	
N20	NC	
N21	IO101NPB1	
N22	IO103PDB1	
P1	NC	
P2	IO199PDB3	
P3	IO199NDB3	
P4	IO202NDB3	
P5	IO202PDB3	
P6	IO196PPB3	
P7	IO193PPB3	
P8	VCCIB3	
P9	GND	
P10	VCC	
P11	VCC	
P12	VCC	
P13	VCC	
P14	GND	
P15	VCCIB1	
P16	GDB0/IO112NPB1	
P17	IO106NDB1	
P18	IO106PDB1	
P19	IO107PDB1	
P20	NC	
P21	IO104PDB1	
P22	IO103NDB1	
R1	NC	
R2	IO197PPB3	
R3	VCC	
R4	IO197NPB3	
R5	IO196NPB3	
R6	IO193NPB3	
R7	GEC0/IO190NPB3	
R8	VMV3	