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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl250v5-fgg144

field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs.

[†] *The AGL015 and AGL030 do not support PLL or SRAM.*

Table 2-39 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS[4]	2 mA	158	164
1.2 V LVCMOS Wide Range[4]	100 μA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*

2. $R_{(PULL-DOWN-MAX)} = (VOLspec) / I_{OLspec}$

3. $R_{(PULL-UP-MAX)} = (VCCImax - VOHspec) / I_{OHspec}$

4. *Applicable to IGLOO V2 Devices operating at VCCI $\geq$ VCC*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

Table 2-47 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Advanced I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-48 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard Plus I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-49 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

3. *Currents are measured at 100°C junction temperature and maximum voltage.*

4. *Currents are measured at 85°C junction temperature.*

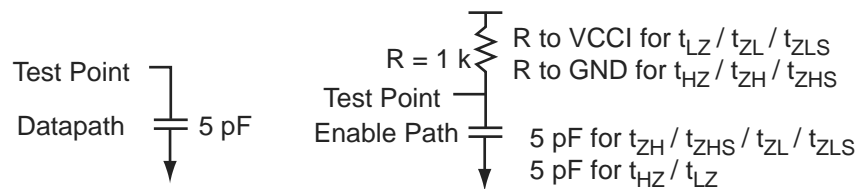5. *Software default selection highlighted in gray.*

Test Point

Datapath ⎓ 5 pF

R = 1 k
Test Point
Enable Path ⎓

R to VCCI for t_{LZ} / t_{ZL} / t_{ZLS}
R to GND for t_{HZ} / t_{ZH} / t_{ZHS}

5 pF for t_{ZH} / t_{ZHS} / t_{ZL} / t_{ZLS}
5 pF for t_{HZ} / t_{LZ}

Figure 2-7 • **AC Loading**

Table 2-50 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

Note: **Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

3.3 V LVCMOS Wide Range

Table 2-63 • **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Advanced I/O Banks**

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 µA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 µA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 µA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 µA	12 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10
100 µA	16 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	132	127	10	10
100 µA	24 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	268	181	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*

2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*

3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

4. *Currents are measured at 100°C junction temperature and maximum voltage.*

5. *Currents are measured at 85°C junction temperature.*

6. *Software default selection highlighted in gray.*

Table 2-71 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
100 µA	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 µA	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-72 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
100 µA	2 mA		0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	4 mA		0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	6 mA		0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 µA	8 mA		0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

3. Software default selection highlighted in gray.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-159 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t$_{OCLKQ}$	Clock-to-Q of the Output Data Register	1.00	ns
t$_{OSUD}$	Data Setup Time for the Output Data Register	0.51	ns
t$_{OHD}$	Data Hold Time for the Output Data Register	0.00	ns
t$_{OSUE}$	Enable Setup Time for the Output Data Register	0.70	ns
t$_{OHE}$	Enable Hold Time for the Output Data Register	0.00	ns
t$_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t$_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
t$_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t$_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t$_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t$_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t$_{OWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t$_{OWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t$_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t$_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-160 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t$_{OCLKQ}$	Clock-to-Q of the Output Data Register	1.52	ns
t$_{OSUD}$	Data Setup Time for the Output Data Register	1.15	ns
t$_{OHD}$	Data Hold Time for the Output Data Register	0.00	ns
t$_{OSUE}$	Enable Setup Time for the Output Data Register	1.11	ns
t$_{OHE}$	Enable Hold Time for the Output Data Register	0.00	ns
t$_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t$_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
t$_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
t$_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
t$_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
t$_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t$_{OWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t$_{OWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
t$_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
t$_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.
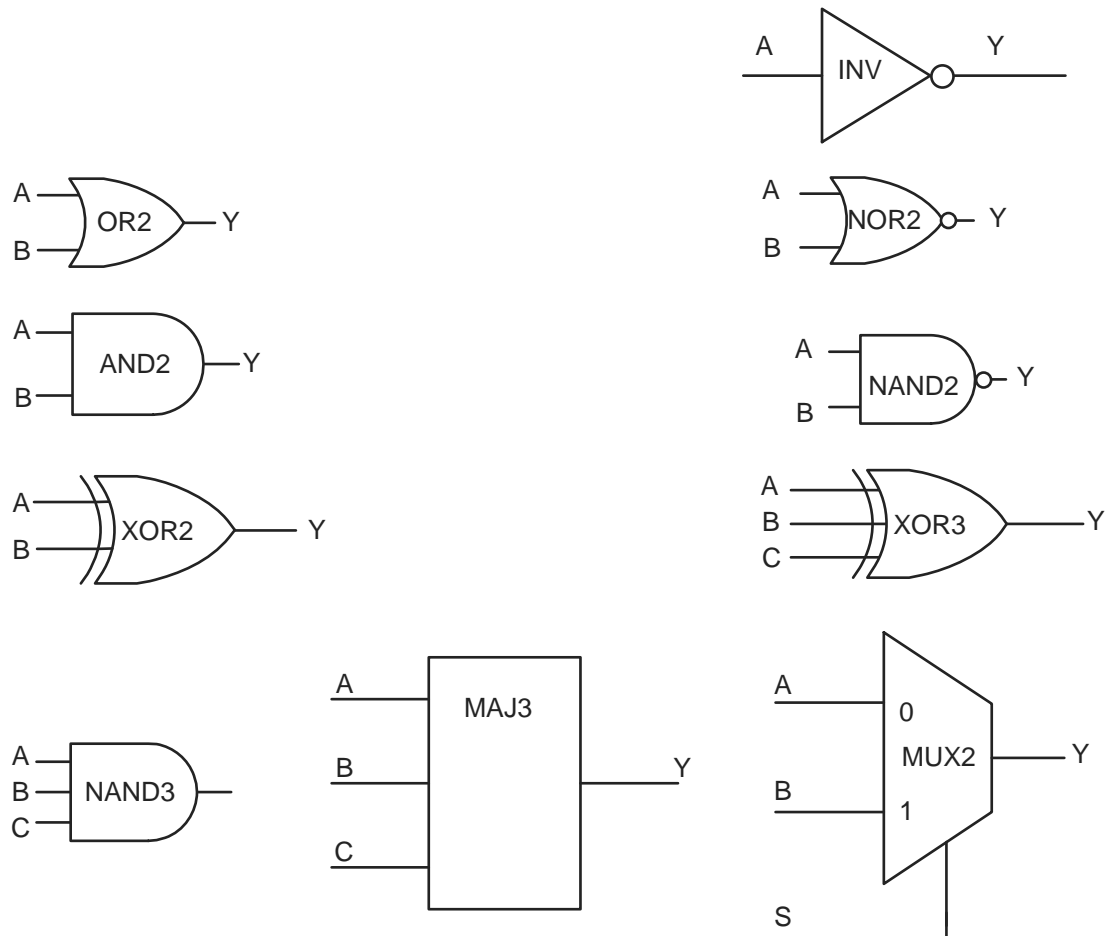

Figure 2-25 • **Sample of Combinatorial Cells**

Table 2-187 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-188 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std. Min.[1]	Std. Max.[2]	Units
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-192 • **RAM512X18**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t$_{AS}$	Address setup time	0.83	ns
t$_{AH}$	Address hold time	0.16	ns
t$_{ENS}$	REN, WEN setup time	0.73	ns
t$_{ENH}$	REN, WEN hold time	0.08	ns
t$_{DS}$	Input data (WD) setup time	0.71	ns
t$_{DH}$	Input data (WD) hold time	0.36	ns
t$_{CKQ1}$	Clock High to new data valid on RD (output retained)	4.21	ns
t$_{CKQ2}$	Clock High to new data valid on RD (pipelined)	1.71	ns
t$_{C2CRWH}$[1]	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
t$_{C2CWRH}$[1]	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.42	ns
t$_{RSTBQ}$	RESET Low to data out Low on RD (flow-through)	2.06	ns
	RESET Low to data out Low on RD (pipelined)	2.06	ns
t$_{REMRSTB}$	RESET removal	0.61	ns
t$_{RECRSTB}$	RESET recovery	3.21	ns
t$_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t$_{CYC}$	Clock cycle time	6.24	ns
F$_{MAX}$	Maximum frequency	160	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

***Table 2-194 •* RAM512X18**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.14 V

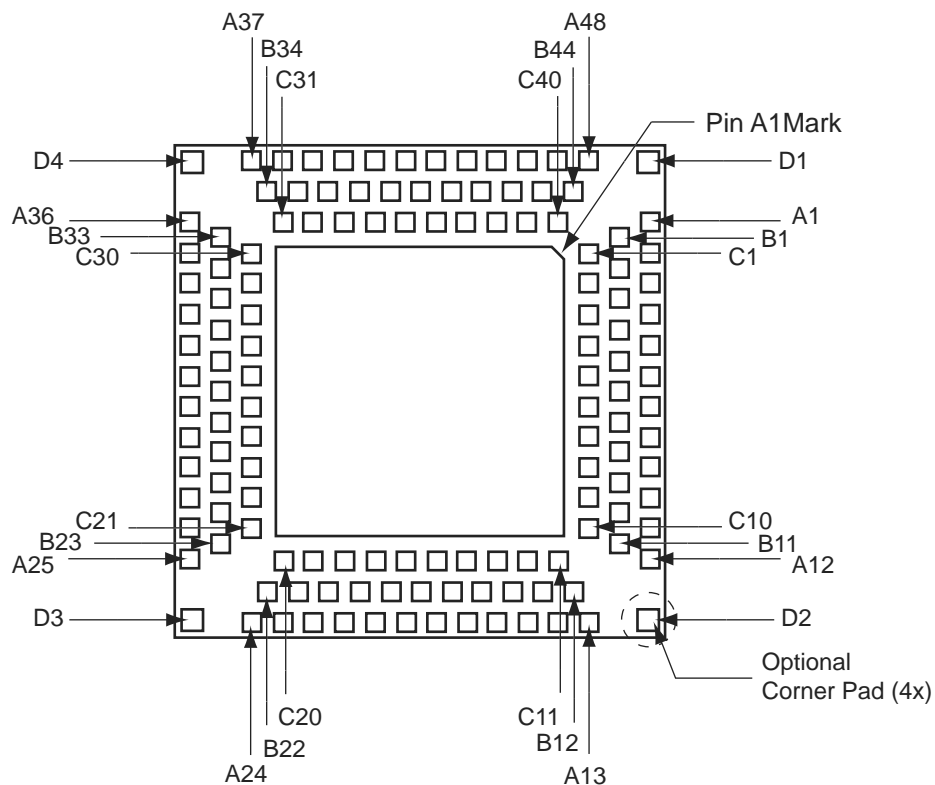| Parameter	Description	Std.	Units
t$_{AS}$	Address setup time	1.53	ns
t$_{AH}$	Address hold time	0.29	ns
t$_{ENS}$	REN, WEN setup time	1.36	ns
t$_{ENH}$	REN, WEN hold time	0.15	ns
t$_{DS}$	Input data (WD) setup time	1.33	ns
t$_{DH}$	Input data (WD) hold time	0.66	ns
t$_{CKQ1}$	Clock High to new data valid on RD (output retained)	7.88	ns
t$_{CKQ2}$	Clock High to new data valid on RD (pipelined)	3.20	ns
t$_{C2CRWH}$[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.87	ns
t$_{C2CWRH}$[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.04	ns
t$_{RSTBQ}$	RESET Low to data out Low on RD (flow through)	3.86	ns
	RESET Low to data out Low on RD (pipelined)	3.86	ns
t$_{REMRSTB}$	RESET removal	1.12	ns
t$_{RECRSTB}$	RESET recovery	5.93	ns
t$_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t$_{CYC}$	Clock cycle time	10.90	ns
F$_{MAX}$	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

UC81		UC81		UC81	
Pin Number	**AGL030 Function**	**Pin Number**	**AGL030 Function**	**Pin Number**	**AGL030 Function**
A1	IO00RSB0	E1	GEB0/IO71RSB1	J1	IO63RSB1
A2	IO02RSB0	E2	GEA0/IO72RSB1	J2	IO61RSB1
A3	IO06RSB0	E3	GEC0/IO73RSB1	J3	IO59RSB1
A4	IO11RSB0	E4	VCCIB1	J4	IO56RSB1
A5	IO16RSB0	E5	VCC	J5	IO52RSB1
A6	IO19RSB0	E6	VCCIB0	J6	IO44RSB1
A7	IO22RSB0	E7	GDC0/IO32RSB0	J7	TCK
A8	IO24RSB0	E8	GDA0/IO33RSB0	J8	TMS
A9	IO26RSB0	E9	GDB0/IO34RSB0	J9	VPUMP
B1	IO81RSB1	F1	IO68RSB1		
B2	IO04RSB0	F2	IO67RSB1		
B3	IO10RSB0	F3	IO64RSB1		
B4	IO13RSB0	F4	GND		
B5	IO15RSB0	F5	VCCIB1		
B6	IO20RSB0	F6	IO47RSB1		
B7	IO21RSB0	F7	IO36RSB0		
B8	IO28RSB0	F8	IO38RSB0		
B9	IO25RSB0	F9	IO40RSB0		
C1	IO79RSB1	G1	IO65RSB1		
C2	IO80RSB1	G2	IO66RSB1		
C3	IO08RSB0	G3	IO57RSB1		
C4	IO12RSB0	G4	IO53RSB1		
C5	IO17RSB0	G5	IO49RSB1		
C6	IO14RSB0	G6	IO45RSB1		
C7	IO18RSB0	G7	IO46RSB1		
C8	IO29RSB0	G8	VJTAG		
C9	IO27RSB0	G9	TRST		
D1	IO74RSB1	H1	IO62RSB1		
D2	IO76RSB1	H2	FF/IO60RSB1		
D3	IO77RSB1	H3	IO58RSB1		
D4	VCC	H4	IO54RSB1		
D5	VCCIB0	H5	IO48RSB1		
D6	GND	H6	IO43RSB1		
D7	IO23RSB0	H7	IO42RSB1		
D8	IO31RSB0	H8	TDI		
D9	IO30RSB0	H9	TDO		

![Microsemi logo]

QN132

Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see *PD3068: Package Mechanical Drawings.*

FG256	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL400 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL400 Function
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

FG484	
Pin Number	**AGL600 Function**
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

FG484	
Pin Number	**AGL600 Function**
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3

FG484	
Pin Number	**AGL600 Function**
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

FG484	
Pin Number	**AGL600 Function**
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	**AGL1000 Function**
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

Revision	Changes	Page
Revision 19	The following figures were deleted (SAR 29991). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 21770).	N/A
	Figure 2-36 • Write Access after Write onto Same Address	
	Figure 2-37 • Read Access after Write onto Same Address	
	Figure 2-38 • Write Access after Read onto Same Address	2-119 to 2-130
	The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-40 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SARs 29991, 30510).	
	The "Pin Descriptions" chapter has been added (SAR 21642).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395).	4-1
	The "CS81" pin table for AGL250 is new (SAR 22737).	4-5
	The CS121 pin table for AGL125 is new (SAR 22737).	
	The P3 function was revised in the "CS196" pin table for AGL250 (SAR 24800).	4-12
	The "QN132" pin table for AGL250 was added.	4-35, 4-42
	The "FG144" pin table for AGL060 was added (SAR 33689)	
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO Device Status" table indicates the status for each device in the device family.	N/A