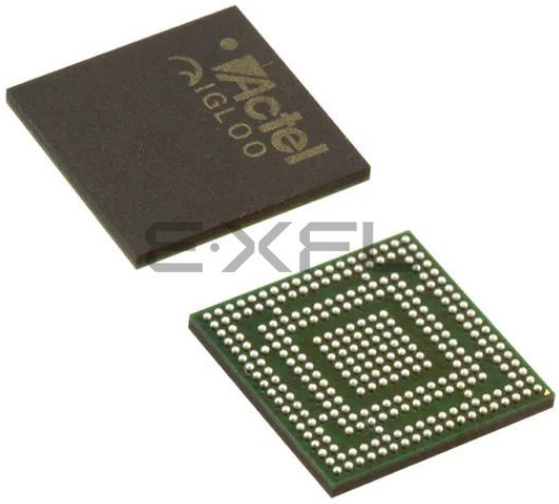

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	215
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	281-TFBGA, CSBGA
Supplier Device Package	281-CSP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl600v2-csg281

User I/O Characteristics

Timing Model

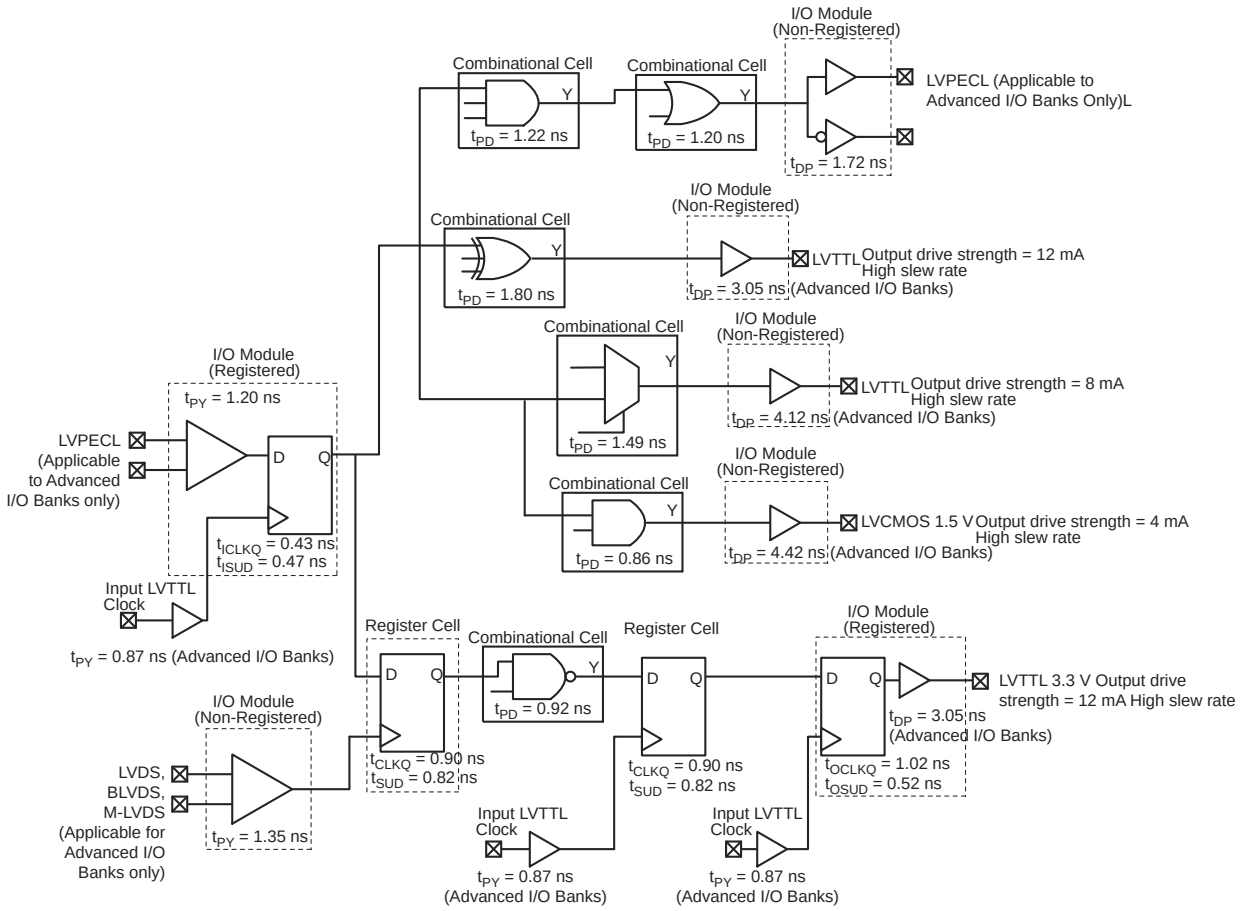

Figure 2-3 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Table 2-35 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard) Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	5	–	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5 V LVCMOS	12 mA	12	High	5	–	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8 V LVCMOS	8 mA	8	High	5	–	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5 V LVCMOS	4 mA	4	High	5	–	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2 V LVCMOS	2 mA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2 V LVCMOS Wide Range[3]	100 µA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3 V PCI	Per PCI spec	–	High	10	25[2]	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[2]	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

3.3 V LVCMOS Wide Range

Table 2-63 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Advanced I/O Banks

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	132	127	10	10
100 µA	24 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	268	181	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-97 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

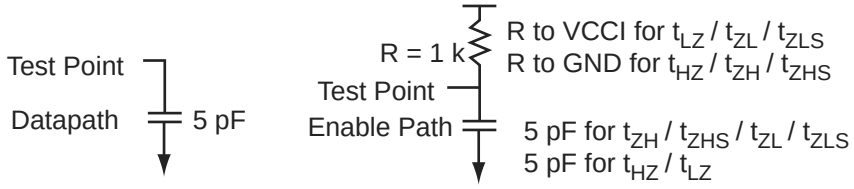

Figure 2-9 • AC Loading

Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-99 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-115* • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

***Table 2-116* • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-117* • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

***Table 2-118* • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Output DDR Module

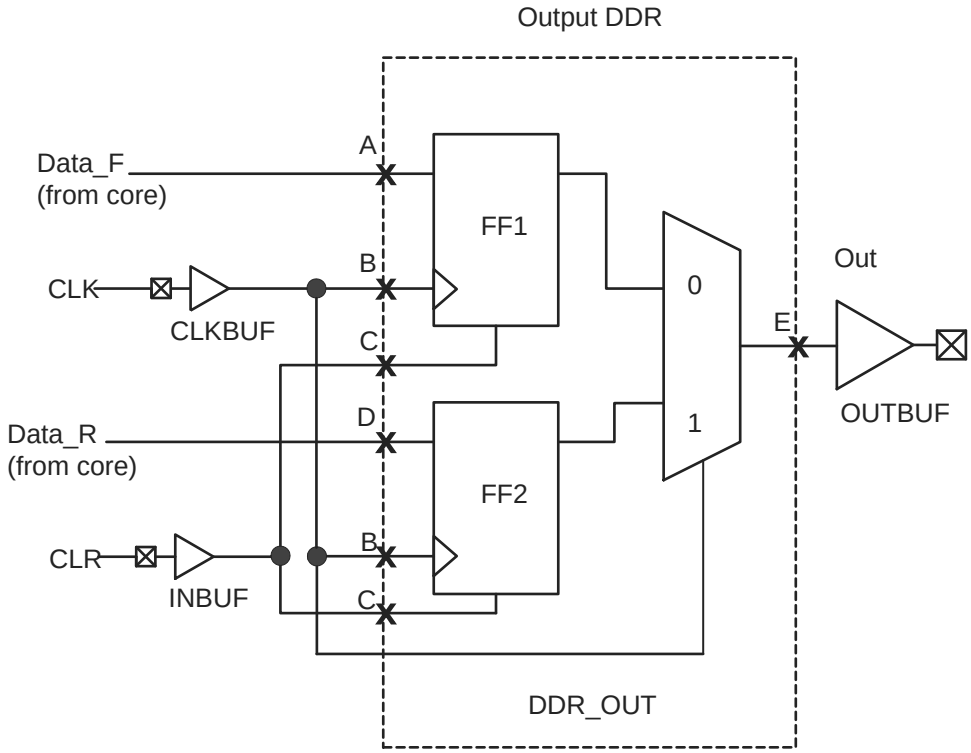

Figure 2-23 • **Output DDR Timing Model**

Table 2-166 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

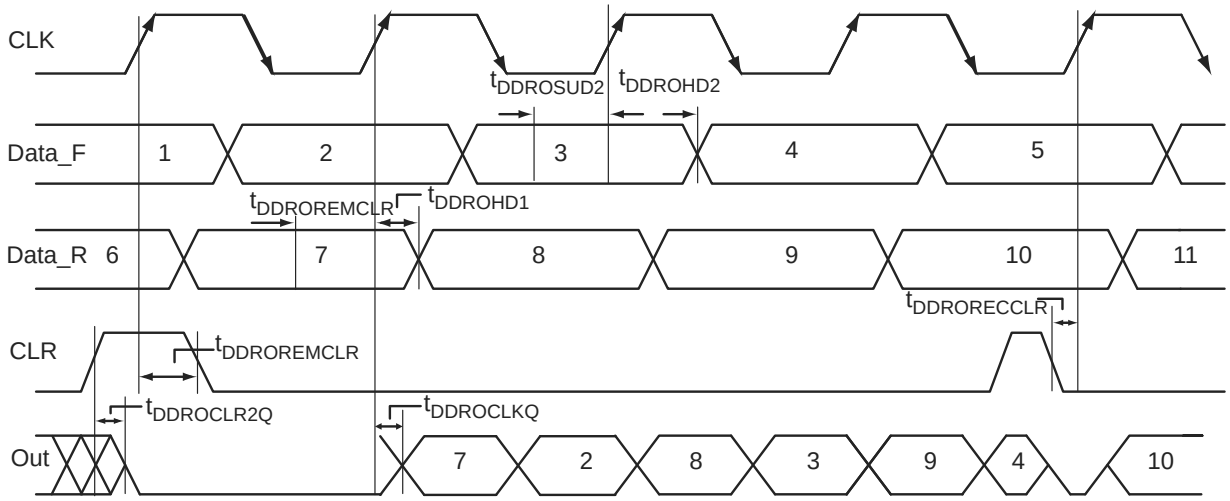

Figure 2-24 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-167 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-187 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-188 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Timing Waveforms

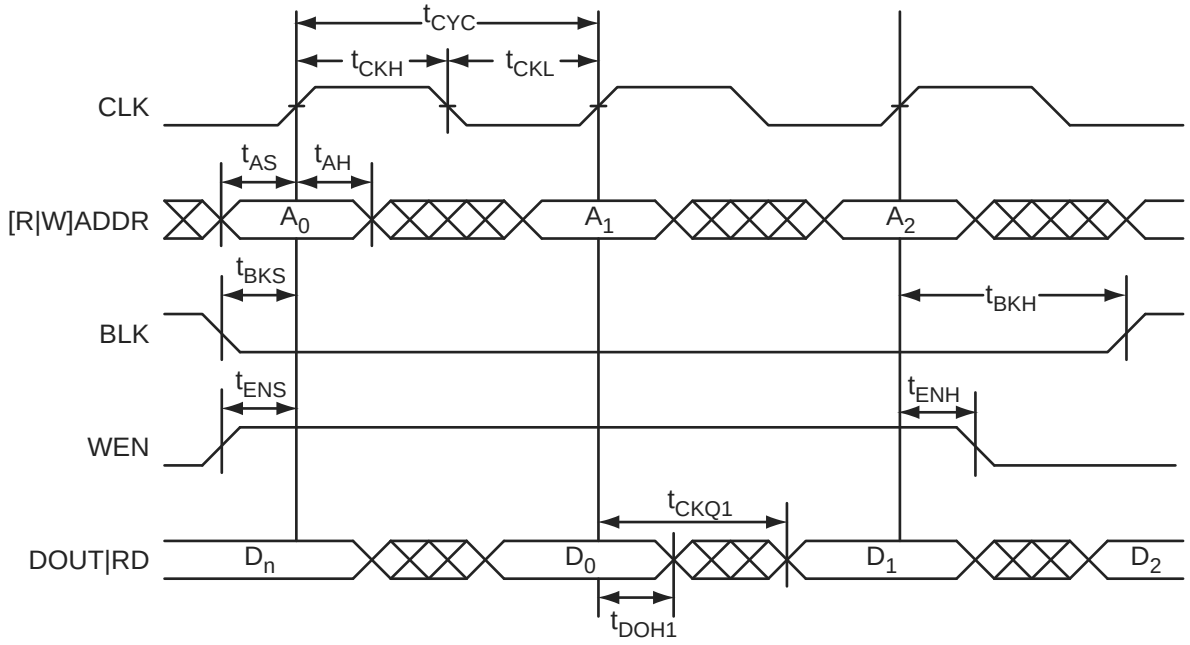

Figure 2-32 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

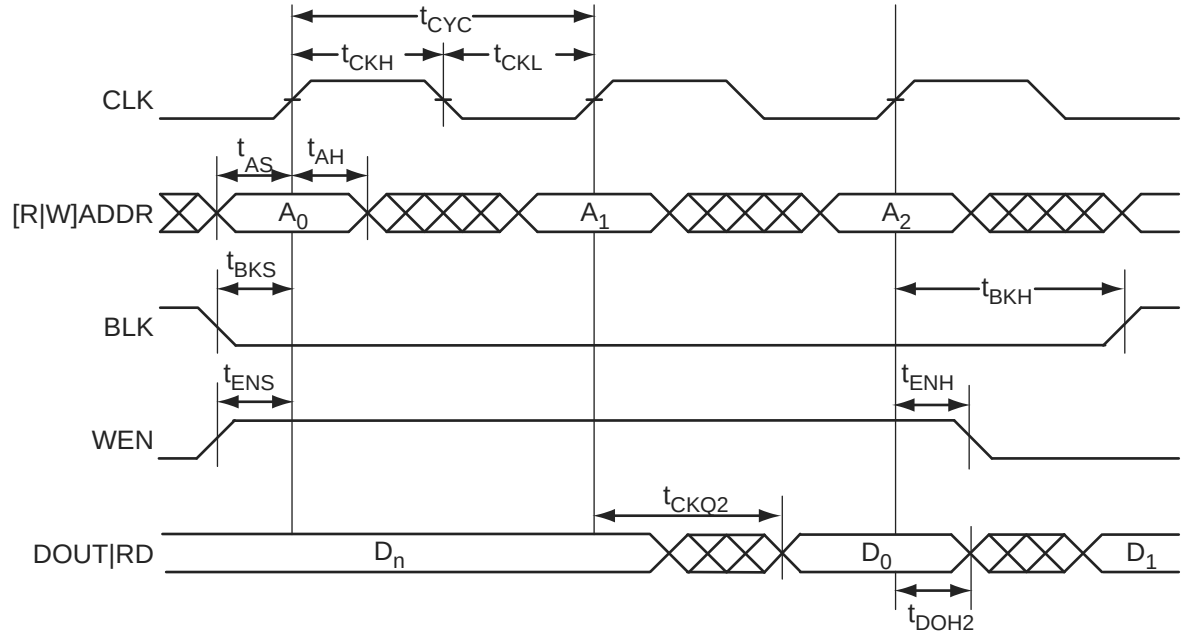

Figure 2-33 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-191 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN, WEN setup time	0.81	ns
t_{ENH}	REN, WEN hold time	0.16	ns
t_{BKS}	BLK setup time	1.65	ns
t_{BKH}	BLK hold time	0.16	ns
t_{DS}	Input data (DIN) setup time	0.71	ns
t_{DH}	Input data (DIN) hold time	0.36	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	3.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	3.06	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.81	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.23	ns
t_{C2CRWL}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	0.41	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	2.06	ns
	RESET Low to data out Low on DOUT (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET removal	0.61	ns
$t_{RECRSTB}$	RESET recovery	3.21	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

CS196	
Pin Number	**AGL125 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	**AGL125 Function**
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	**AGL125 Function**
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

CS196	
Pin Number	**AGL125 Function**
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	VCC
J8	VCC
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	VCCIB1
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	VCCIB0
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1

CS196	
Pin Number	**AGL125 Function**
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	VPUMP
L12	VJTAG
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	VCCIB1
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	VCCIB1
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	VCCIB1
M12	VMV1
M13	TRST
M14	VCCIB0
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI

CS196	
Pin Number	**AGL125 Function**
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

QN132	
Pin Number	**AGL125 Function**
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

VQ100	
Pin Number	**AGL250 Function**
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	**AGL250 Function**
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	**AGL250 Function**
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

FG484	
Pin Number	**AGL400 Function**
G5	IO151UDB3
G6	GAC2/IO153UDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO46RSB0
G15	GNDQ
G16	IO47RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO150PDB3
H5	IO08RSB0
H6	IO153VDB3
H7	IO152VDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO65RSB1
H18	IO52RSB0

FG484	
Pin Number	**AGL400 Function**
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO150NDB3
J5	IO149NPB3
J6	IO09RSB0
J7	IO152UDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO49RSB0
J18	IO64PPB1
J19	IO66NDB1
J20	NC
J21	NC
J22	NC
K1	NC
K2	NC
K3	NC
K4	IO148NDB3
K5	IO148PDB3
K6	IO149PPB3
K7	GFC1/IO147PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	**AGL400 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO67PPB1
K17	IO64NPB1
K18	IO73PDB1
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC

FG484	
Pin Number	**AGL600 Function**
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1

Revision / Version	Changes	Page
Revision 3 (Feb 2008) Product Brief rev. 2	This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following sections were updated: "Features and Benefits" "IGLOO Ordering Information" "Temperature Grade Offerings" "IGLOO Devices" Product Family Table Table 1 • IGLOO FPGAs Package Sizes Dimensions "AGL015 and AGL030" note	N/A
	The "Temperature Grade Offerings" table was updated to include M1AGL600.	IV
	In the "IGLOO Ordering Information" table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm.	III
	In the "General Description" section, the number of I/Os was updated from 288 to 300.	1-1
Packaging v1.2	The "QN68" section is new.	4-25
Revision 2 (Jan 2008) Packaging v1.1	The "CS196" package and pin table was added for AGL125.	4-10
Revision 1 (Jan 2008) Product Brief rev. 1	The "Low Power" section was updated to change the description of low power active FPGA operation to "from 12 µW" from "from 25 µW." The same update was made in the "General Description" section and the "Flash*Freeze Technology" section.	I, 1-1
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the numbering.	N/A
Advance v0.7 (December 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000.	i, ii, iv
	Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table.	ii
	The "I/Os Per Package1"table was updated to reflect 77 instead of 79 single-ended I/Os for the VG100 package for AGL030.	ii
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-20
	In Table 2-27 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, T_J was changed to T_A in notes 1 and 2.	2-26
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-74
	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1.	N/A
	Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated.	2-19, 2-20

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

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This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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