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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	177
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1agl600v2-fg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 2-39 • I/O Output Buffer Maximum Resistances¹ Applicable to Standard Plus I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS ⁴	2 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

2. R_(PULL-DOWN-MAX) = (VOLspec) / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / I_{OHspec}

4. Applicable to IGLOO V2 Devices operating at VCCI \geq VCC

^{1.} These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

Table 2-44 • I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16
1.2 V LVCMOS	1 mA	20	26
1.2 V LVCMOS Wide Range	100 μA	20	26

Note: $^{*}T_{J} = 100^{\circ}C$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-45 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
-40°C	> 20 years
–20°C	> 20 years
O°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (100°C)
LVDS/B-LVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

Note: The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	v	1L	v	IH	VOL	VОН	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Table 2-79 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

 Table 2-80 •
 Minimum and Maximum DC Input and Output Levels

 Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	v	ΊL	v	ΊH	VOL	vон	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Applies to 1.2 V Core Voltage

Table 2-89 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-91 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-119 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-120 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-121 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-122 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

Table 2-127 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.2 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

- 2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 3. Currents are measured at 100°C junction temperature and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Table 2-128 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.2 V LVCMOS		VIL	VIH		VOL	VOH	I _{OL}	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

- 1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
- 2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 3. Currents are measured at 100°C junction temperature and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Table 2-129 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.2 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
1 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at 100°C junction temperature and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

I/O Register Specifications



Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-16 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
tOSUD	Data Setup Time for the Output Data Register	F, H
t _{OHD}	Data Hold Time for the Output Data Register	F, H
t _{OSUE}	Enable Setup Time for the Output Data Register	G, H
t _{OHE}	Enable Hold Time for the Output Data Register	G, H
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
tOESUD	Data Setup Time for the Output Enable Register	J, H
t _{OEHD}	Data Hold Time for the Output Enable Register	J, H
tOESUE	Enable Setup Time for the Output Enable Register	K, H
t _{OEHE}	Enable Hold Time for the Output Enable Register	К, Н
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t _{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t _{ISUD}	Data Setup Time for the Input Data Register	C, A
t _{IHD}	Data Hold Time for the Input Data Register	C, A
t _{ISUE}	Enable Setup Time for the Input Data Register	B, A
t _{IHE}	Enable Hold Time for the Input Data Register	B, A
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
tIRECPRE	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Table 2-155 • Parameter Definition and Measuring Nodes

Note: *See Figure 2-16 on page 2-84 for more information.

VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.



Figure 2-27 • Sample of Sequential Cells

Table 2-190 • IGLOO CCC/PLL Specification For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Тур.	Max.	Units
Clock Conditioning Circuitry Input Frequency fIN_CCC	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f _{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks ^{1,2}		580 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{4,5}			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁶				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1,2}	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 ^{1,2}	0.863		20.86	ns
Delay Range in Block: Fixed Delay ^{1, 2, 5}		5.7		ns
CCC Output Peak-to-Peak Period Jitter F _{CCC_OUT}	Maxim	um Peak-to-F	Peak Jitter Dat	a ^{7,8}
	$SSO \geq 4^9$	$SSO \geq 8^9$	$SSO \geq 16^9$	
0.75 MHz to 50 MHz	1.20%	2.00%	3.00%	
50 MHz to 160 MHz	5.00%	7.00%	15.00%	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.

2. $T_J = 25^{\circ}C$, $V_{CC} = 1.2 V$

3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

5. The AGL030 device does not support a PLL.

6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

7. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.

Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.

 SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.

10. For definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the IGLOO FPGA Fabric User Guide.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-191 • RAM4K9

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t _{AS}	Address setup time	0.83	ns
t _{AH}	Address hold time	0.16	ns
t _{ENS}	REN, WEN setup time	0.81	ns
t _{ENH}	REN, WEN hold time	0.16	ns
t _{BKS}	BLK setup time	1.65	ns
t _{BKH}	BLK hold time	0.16	ns
t _{DS}	Input data (DIN) setup time	0.71	ns
t _{DH}	Input data (DIN) hold time	0.36	ns
t _{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	3.53	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	3.06	ns
t _{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.81	ns
t _{C2CWWL} 1	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.23	ns
t _{C2CRWL} 1	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.35	ns
t _{C2CWRH} 1	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	0.41	ns
t _{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	2.06	ns
	RESET Low to data out Low on DOUT (pipelined)	2.06	ns
t _{REMRSTB}	RESET removal	0.61	ns
t _{RECRSTB}	RESET recovery	3.21	ns
t _{MPWRSTB}	RESET minimum pulse width	0.68	ns
t _{CYC}	Clock cycle time	6.24	ns
F _{MAX}	Maximum frequency	160	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

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Package Pin Assignments

	CS196		CS196		CS196
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GND	C8	IO31RSB0	F2	IO144NPB3
A2	GAA0/IO00RSB0	C9	IO44RSB0	F3	IO148PDB3
A3	GAC0/IO04RSB0	C10	IO49RSB0	F4	IO148NDB3
A4	GAC1/IO05RSB0	C11	VCCIB0	F5	IO150NPB3
A5	IO14RSB0	C12	IO60NPB1	F6	IO07RSB0
A6	IO18RSB0	C13	GNDQ	F7	VCC
A7	IO26RSB0	C14	IO61NDB1	F8	VCC
A8	IO29RSB0	D1	IO153VDB3	F9	IO43RSB0
A9	IO36RSB0	D2	IO154VDB3	F10	IO73PDB1
A10	GBC0/IO54RSB0	D3	GAA2/IO155UDB3	F11	IO73NDB1
A11	GBB0/IO56RSB0	D4	IO150PPB3	F12	IO66NDB1
A12	GBB1/IO57RSB0	D5	IO11RSB0	F13	IO66PDB1
A13	GBA1/IO59RSB0	D6	IO20RSB0	F14	IO64NDB1
A14	GND	D7	IO23RSB0	G1	GFB1/IO146PDB3
B1	VCCIB3	D8	IO28RSB0	G2	GFA0/IO145NDB3
B2	VMV0	D9	IO41RSB0	G3	GFA2/IO144PPB3
B2	VMV0	D10	IO47RSB0	G4	VCOMPLF
B3	GAA1/IO01RSB0	D11	IO63PPB1	G5	GFC0/IO147NDB3
B4	GAB1/IO03RSB0	D12	VMV1	G6	VCC
B5	GND	D13	IO62NDB1	G7	GND
B6	IO17RSB0	D14	GBC2/IO62PDB1	G8	GND
B7	IO25RSB0	E1	IO149PDB3	G9	VCC
B8	IO34RSB0	E2	GND	G10	GCC0/IO67NDB1
B9	IO39RSB0	E3	IO155VDB3	G11	GCB1/IO68PDB1
B10	GND	E4	VCCIB3	G12	GCA0/IO69NDB1
B11	GBC1/IO55RSB0	E5	IO151USB3	G13	IO72NDB1
B12	GBA0/IO58RSB0	E6	IO09RSB0	G14	GCC2/IO72PDB1
B13	GBA2/IO60PPB1	E7	IO12RSB0	H1	GFB0/IO146NDB3
B14	GBB2/IO61PDB1	E8	IO32RSB0	H2	GFA1/IO145PDB3
C1	GAC2/IO153UDB3	E9	IO46RSB0	H3	VCCPLF
C2	GAB2/IO154UDB3	E10	IO51RSB0	H4	GFB2/IO143PPB3
C3	GNDQ	E11	VCCIB1	H5	GFC1/IO147PDB3
C4	VCCIB0	E12	IO63NPB1	H6	VCC
C5	GAB0/IO02RSB0	E13	GND	H7	GND
C6	IO15RSB0	E14	IO64PDB1	H8	GND
C7	VCCIB0	F1	IO149NDB3	H9	VCC

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IGLOO Low Power Flash FPGAs

	QN132		QN132		QN132
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
A1	GAB2/IO69RSB1	A37	GBB1/IO38RSB0	B25	GND
A2	IO130RSB1	A38	GBC0/IO35RSB0	B26	NC
A3	VCCIB1	A39	VCCIB0	B27	GCB2/IO58RSB0
A4	GFC1/IO126RSB1	A40	IO28RSB0	B28	GND
A5	GFB0/IO123RSB1	A41	IO22RSB0	B29	GCB0/IO54RSB0
A6	VCCPLF	A42	IO18RSB0	B30	GCC1/IO51RSB0
A7	GFA1/IO121RSB1	A43	IO14RSB0	B31	GND
A8	GFC2/IO118RSB1	A44	IO11RSB0	B32	GBB2/IO43RSB0
A9	IO115RSB1	A45	IO07RSB0	B33	VMV0
A10	VCC	A46	VCC	B34	GBA0/IO39RSB0
A11	GEB1/IO110RSB1	A47	GAC1/IO05RSB0	B35	GBC1/IO36RSB0
A12	GEA0/IO107RSB1	A48	GAB0/IO02RSB0	B36	GND
A13	GEC2/IO104RSB1	B1	IO68RSB1	B37	IO26RSB0
A14	IO100RSB1	B2	GAC2/IO131RSB1	B38	IO21RSB0
A15	VCC	B3	GND	B39	GND
A16	IO99RSB1	B4	GFC0/IO125RSB1	B40	IO13RSB0
A17	IO96RSB1	B5	VCOMPLF	B41	IO08RSB0
A18	IO94RSB1	B6	GND	B42	GND
A19	IO91RSB1	B7	GFB2/IO119RSB1	B43	GAC0/IO04RSB0
A20	IO85RSB1	B8	IO116RSB1	B44	GNDQ
A21	IO79RSB1	B9	GND	C1	GAA2/IO67RSB1
A22	VCC	B10	GEB0/IO109RSB1	C2	IO132RSB1
A23	GDB2/IO71RSB1	B11	VMV1	C3	VCC
A24	TDI	B12	FF/GEB2/IO105RSB1	C4	GFB1/IO124RSB1
A25	TRST	B13	IO101RSB1	C5	GFA0/IO122RSB1
A26	GDC1/IO61RSB0	B14	GND	C6	GFA2/IO120RSB1
A27	VCC	B15	IO98RSB1	C7	IO117RSB1
A28	IO60RSB0	B16	IO95RSB1	C8	VCCIB1
A29	GCC2/IO59RSB0	B17	GND	C9	GEA1/IO108RSB1
A30	GCA2/IO57RSB0	B18	IO87RSB1	C10	GNDQ
A31	GCA0/IO56RSB0	B19	IO81RSB1	C11	GEA2/IO106RSB1
A32	GCB1/IO53RSB0	B20	GND	C12	IO103RSB1
A33	IO49RSB0	B21	GNDQ	C13	VCCIB1
A34	VCC	B22	TMS	C14	IO97RSB1
A35	IO44RSB0	B23	TDO	C15	IO93RSB1
A36	GBA2/IO41RSB0	B24	GDC0/IO62RSB0	C16	IO89RSB1

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Pin Number	AGL600 Function					
R9	VCCIB2					
R10	VCCIB2					
R11	IO117RSB2					
R12	IO110RSB2					
R13	VCCIB2					
R14	VCCIB2					
R15	VMV2					
R16	IO94RSB2					
R17	GDB1/IO87PPB1					
R18	GDC1/IO86PDB1					
R19	IO84NDB1					
R20	VCC					
R21	IO81NDB1					
R22	IO82PDB1					
T1	IO152PDB3					
T2	IO152NDB3					
Т3	NC					
T4	IO150NDB3					
T5	IO147PPB3					
Т6	GEC1/IO146PPB3					
T7	IO140RSB2					
Т8	GNDQ					
Т9	GEA2/IO143RSB2					
T10	IO126RSB2					
T11	IO120RSB2					
T12	IO108RSB2					
T13	IO103RSB2					
T14	IO99RSB2					
T15	GNDQ					
T16	IO92RSB2					
T17	VJTAG					
T18	GDC0/IO86NDB1					
T19	GDA1/IO88PDB1					
T20	NC					
T21	IO83PDB1					
T22	IO82NDB1					

	FG484
Pin Number	AGL1000 Function
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3

5 – Datasheet Information

List of Changes

The following tables list critical changes that were made in each revision of the IGLOO datasheet.

Revision	Changes	Page
Revision 27 (May 2016)	Added the deleted package FG144 from AGL125 device in "IGLOO Devices" (SAR 79355).	1-I
Revision 26 (March 2016)	 Updated "IGLOO Ordering Information" and "Temperature Grade Offerings" notes by: Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352). Replacing Industrial (-40°C to +85°C Ambient Temperature) with Industrial (-40°C to +100°C Junction Temperature) (SAR 48352). 	1-III and 1-IV
	Ambient temperature row removed in Table 2-2 (SAR 48352).	2-2
	Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087).	2-2
	Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087)	2-2
	Added 2 mA drive strengths in tables same as 4 mA (SAR 57179).	NA
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777).	NA
Revision 25 (June2015)	Removed package FG144 from AGL060 device in the following tables: "IGLOO Devices", "I/Os Per Package1" and "Temperature Grade Offerings" (SAR 68517)	I, II, and IV
	Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517)	-
Revision 24 (March 2014)	Note added for the discontinuance of QN132 package to the following tables: "IGLOO Devices", "I/Os Per Package1", "IGLOO FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings" and "QN132" section (SAR 55117, PDN 1306).	I, II, IV, and 4-28
	Removed packages CS81 and QN132 from AGL250 device in the following tables: "IGLOO Devices", "I/Os Per Package1", and "Temperature Grade Offerings" (SAR 49472).	I, II, and IV

IGLOO Low Power Flash FPGAs

Revision / Version	Changes	Page
DC & Switching, cont'd.	Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.	2-39
Revision 9 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change $1.2 \text{ V} / 1.5 \text{ V}$ to 1.2 V to 1.5 V .	N/A
Revision 8 (Jun 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change $1.2 \text{ V} / 1.5 \text{ V}$ to 1.2 V to 1.5 V .	N/A
DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time.	N/A
	The power data table has been updated to match SmartPower data rather then simulation values. AGL015 global clock delays have been added.	
	Table 2-1 • Absolute Maximum Ratings was updated to combine the VCCI and VMV parameters in one row. The word "output" from the parameter description for VCCI and VMV, and table note 3 was added.	2-1
	Table 2-2 • Recommended Operating Conditions 1 was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the VCCI parameter row, and table note 9 was added.	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-3
	VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new.	2-5
	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode*, Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*, and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode1 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-9



Datasheet Information

Revision / Version	Changes	Page
Revision 8 (cont'd)	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, and Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 were updated to change PDC2 to PDC6 and PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI.	2-10 through 2-11
	In Table 2-19 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices, the description for PAC13 was changed from Static to Dynamic.	2-13
	Table 2-20 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-22 • Different Components Contributing to the Static Power Consumption in IGLOO Device were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power. Subtitles were added to indicate type of devices and core supply voltage.	2-14, 2-16
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P _{STAT} , including PDC6 and PDC7.	2-17
	Footnote † was updated to include information about PAC13. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-18
Revision 7 (Jun 2008) Packaging v1.5	The "QN132" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-28
Revision 6 (Jun 2008) Packaging v1.4	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	Pin numbers were added to the "QN68" package diagram. Note 2 was added below the diagram.	4-25
Revision 5 (Mar 2008) Packaging v1.3	The "CS196" package and pin table was added for AGL250.	4-12
Revision 4 (Mar 2008) Product Brief v1.0	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 12 μ W)" was removed from "Low Power Active FPGA Operation."	Ι
	1.2_V was added to the list of core and I/O voltages in the "Advanced I/O" and "I/Os with Advanced I/O Standards" section sections.	l, 1-7
	The "Embedded Memory" section was updated to remove the footnote reference from the section heading and place it instead after "4,608-Bit" and "True Dual-Port SRAM (except ×18)."	I

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IGLOO Low Power Flash FPGAs

Revision / Version	Changes	Page
Revision 3 (Feb 2008) Product Brief rev. 2	This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following sections were updated: "Features and Benefits"	N/A
	"IGLOO Ordering Information"	
	"Temperature Grade Offerings"	
	"IGLOO Devices" Product Family Table	
	Table 1 • IGLOO FPGAs Package Sizes Dimensions	
	"AGL015 and AGL030" note	
	The "Temperature Grade Offerings" table was updated to include M1AGL600.	IV
	In the "IGLOO Ordering Information" table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm.	
	In the "General Description" section, the number of I/Os was updated from 288 to 300.	1-1
Packaging v1.2	The "QN68" section is new.	4-25
Revision 2 (Jan 2008)	The "CS196" package and pin table was added for AGL125.	4-10
Packaging v1.1		
Revision 1 (Jan 2008) Product Brief rev. 1	The "Low Power" section was updated to change the description of low power active FPGA operation to "from 12 μ W" from "from 25 μ W." The same update was made in the "General Description" section and the "Flash*Freeze Technology" section.	I, 1-1
Revision 0 (Jan 2008)	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the numbering.	N/A
Advance v0.7 (December 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000.	i, ii, iv
	Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table.	ii
	The "I/Os Per Package1"table was updated to reflect 77 instead of 79 single- ended I/Os for the VG100 package for AGL030.	ii
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-20
	In Table 2-27 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, T_J was changed to T_A in notes 1 and 2.	2-26
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-74
	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1.	N/A
	Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated.	2-19, 2-20

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo, CA 92656 USA Within the USA: +1 (800) 713-4113 Outside the USA: +1 (949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996 E-mail: sales.support@microsemi.com www.microsemi.com

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