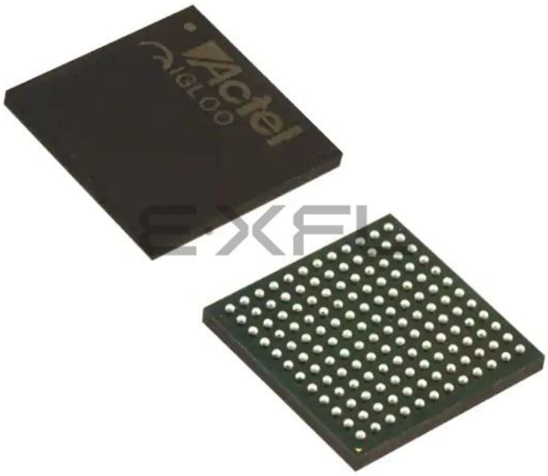


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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 13824 |
| Total RAM Bits | 110592 |
| Number of I/O | 97 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1agl600v2-fgg144 |

## Overview of I/O Performance

### *Summary of I/O DC Input and Output Levels – Default I/O Software Settings*

**Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**
**Applicable to Advanced I/O Banks**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[2] | Slew Rate | VIL | | VIH | | VOL | VOH | IOL[1] | IOH[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min.V | Max. V | Min. V | Max.V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3 V LVCMOS Wide Range[3] | 100 µA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 0.1 | 0.1 |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 1.2 V LVCMOS[4] | 2 mA | 2 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.26 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 |
| 1.2 V LVCMOS Wide Range[4,5] | 100 µA | 2 mA | High | –0.3 | 0.3 * VCCI | 0.7 * VCCI | 1.575 | 0.1 | VCCI – 0.1 | 0.1 | 0.1 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | | |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

## Summary of I/O Timing Characteristics – Default I/O Software Settings

***Table 2-29 •*** **Summary of AC Measuring Points**

| Standard | Measuring Trip Point (Vtrip) |
|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 1.4 V |
| 3.3 V VCMOS Wide Range | 1.4 V |
| 2.5 V LVCMOS | 1.2 V |
| 1.8 V LVCMOS | 0.90 V |
| 1.5 V LVCMOS | 0.75 V |
| 1.2 V LVCMOS | 0.60 V |
| 1.2 V LVCMOS Wide Range | 0.60 V |
| 3.3 V PCI | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |
| 3.3 V PCI-X | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |

***Table 2-30 •*** **I/O AC Parameter Definitions**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

***Table 2-44 •*** **I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| 1.2 V LVCMOS | 1 mA | 20 | 26 |
| 1.2 V LVCMOS Wide Range | 100 µA | 20 | 26 |

*Note:* *$*T_J = 100°C$*

The length of time an I/O can withstand $I_{OSH}/I_{OSL}$ events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-45 •*** **Duration of Short Circuit Event before Failure**

| Temperature | Time before Failure |
|---|---|
| –40°C | > 20 years |
| –20°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |

***Table 2-46 •*** **I/O Input Rise Time, Fall Time, and Related I/O Reliability1**

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS | No requirement | 10 ns * | 20 years (100°C) |
| LVDS/B-LVDS/M-LVDS/ LVPECL | No requirement | 10 ns * | 10 years (100°C) |

*Note: The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

**Table 2-65 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard I/O Banks**

| 3.3 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

**Table 2-66 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

**Table 2-75 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 Applicable to Standard Plus Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 1.55 | 6.69 | 0.26 | 1.32 | 1.10 | 6.69 | 5.73 | 3.41 | 3.72 | 12.48 | 11.52 | ns |
| 100 µA | 4 mA | Std. | 1.55 | 6.69 | 0.26 | 1.32 | 1.10 | 6.69 | 5.73 | 3.41 | 3.72 | 12.48 | 11.52 | ns |
| 100 µA | 6 mA | Std. | 1.55 | 5.58 | 0.26 | 1.32 | 1.10 | 5.58 | 5.01 | 3.77 | 4.35 | 11.36 | 10.79 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 5.58 | 0.26 | 1.32 | 1.10 | 5.58 | 5.01 | 3.77 | 4.35 | 11.36 | 10.79 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 4.82 | 0.26 | 1.32 | 1.10 | 4.82 | 4.44 | 4.02 | 4.76 | 10.61 | 10.23 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 4.82 | 0.26 | 1.32 | 1.10 | 4.82 | 4.44 | 4.02 | 4.76 | 10.61 | 10.23 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

**Table 2-76 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7 Applicable to Standard Plus Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 1.55 | 4.10 | 0.26 | 1.32 | 1.10 | 4.10 | 3.30 | 3.40 | 3.92 | 9.89 | 9.09 | ns |
| 100 µA | 4 mA | Std. | 1.55 | 4.10 | 0.26 | 1.32 | 1.10 | 4.10 | 3.30 | 3.40 | 3.92 | 9.89 | 9.09 | ns |
| 100 µA | 6 mA | Std. | 1.55 | 3.51 | 0.26 | 1.32 | 1.10 | 3.51 | 2.79 | 3.76 | 4.56 | 9.30 | 8.57 | ns |
| 100 µA | 8 mA | Std. | 1.55 | 3.51 | 0.26 | 1.32 | 1.10 | 3.51 | 2.79 | 3.76 | 4.56 | 9.30 | 8.57 | ns |
| 100 µA | 12 mA | Std. | 1.55 | 3.20 | 0.26 | 1.32 | 1.10 | 3.20 | 2.52 | 4.01 | 4.97 | 8.99 | 8.31 | ns |
| 100 µA | 16 mA | Std. | 1.55 | 3.20 | 0.26 | 1.32 | 1.10 | 3.20 | 2.52 | 4.01 | 4.97 | 8.99 | 8.31 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

***Table 2-113 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | μA[4] | μA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

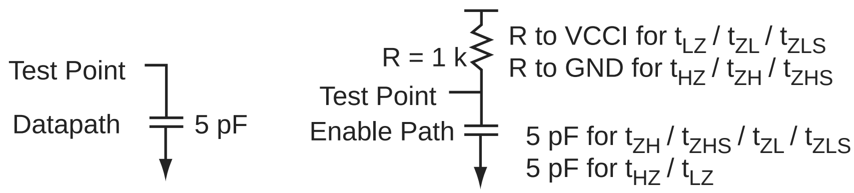



***Figure 2-10 •*** **AC Loading**

***Table 2-114 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 1.5 | 0.75 | 5 |

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

***Table 2-123* • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 6.43 | 0.26 | 1.27 | 1.10 | 6.54 | 5.95 | 2.82 | 2.83 | 12.32 | 11.74 | ns |
| 4 mA | Std. | 1.55 | 5.59 | 0.26 | 1.27 | 1.10 | 5.68 | 5.27 | 3.07 | 3.27 | 11.47 | 11.05 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-124* • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.02 | 0.26 | 1.27 | 1.10 | 3.07 | 2.81 | 2.82 | 2.92 | 8.85 | 8.59 | ns |
| 4 mA | Std. | 1.55 | 2.68 | 0.26 | 1.27 | 1.10 | 2.72 | 2.39 | 3.07 | 3.37 | 8.50 | 8.18 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-125* • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 6.35 | 0.26 | 1.22 | 1.10 | 6.46 | 5.93 | 2.40 | 2.46 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-126* • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 2.92 | 0.26 | 1.22 | 1.10 | 2.96 | 2.60 | 2.40 | 2.56 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Input Register

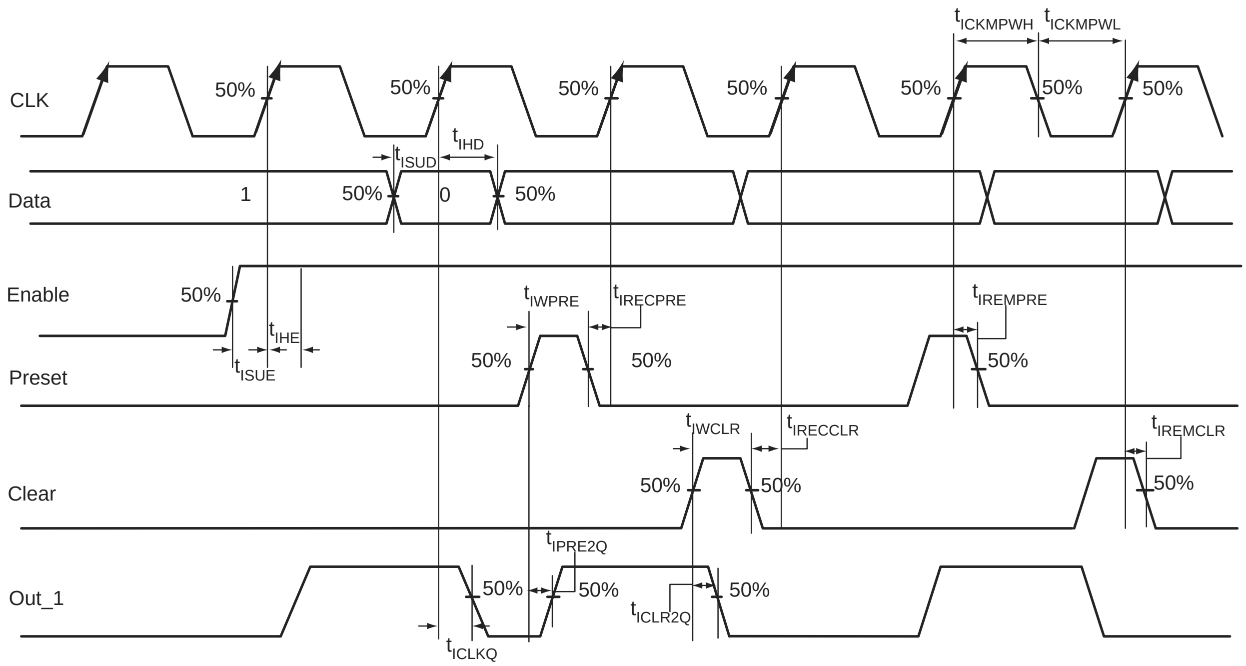



***Figure 2-18 •*** **Input Register Timing Diagram**

### *Timing Characteristics*

#### *1.5 V DC Core Voltage*

***Table 2-157 •*** **Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.42 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.47 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.67 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.79 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-191 • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.83 | ns |
| $t_{AH}$ | Address hold time | 0.16 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.81 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.16 | ns |
| $t_{BKS}$ | BLK setup time | 1.65 | ns |
| $t_{BKH}$ | BLK hold time | 0.16 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.71 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.36 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 3.53 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 3.06 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 1.81 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge | 0.23 | ns |
| $t_{C2CRWL}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge | 0.35 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge | 0.41 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 2.06 | ns |
| | RESET Low to data out Low on DOUT (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

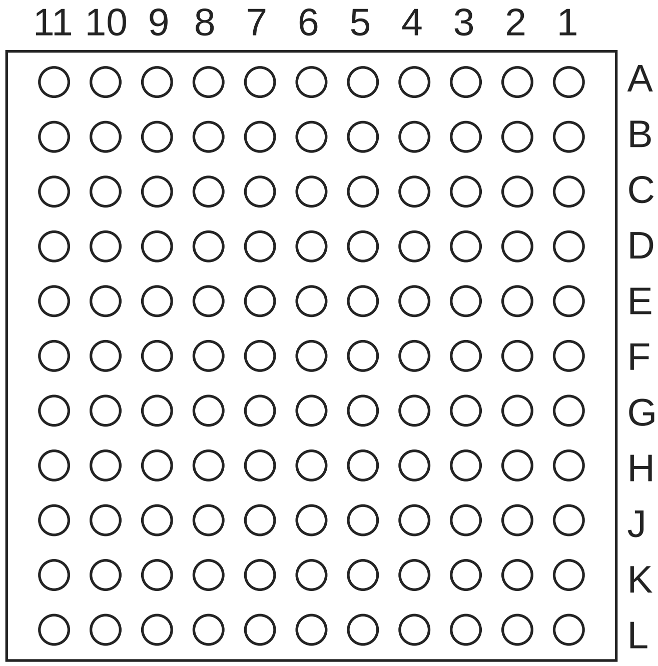
**Table 2-194 • RAM512X18**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 1.53 | ns |
| $t_{AH}$ | Address hold time | 0.29 | ns |
| $t_{ENS}$ | REN, WEN setup time | 1.36 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.15 | ns |
| $t_{DS}$ | Input data (WD) setup time | 1.33 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.66 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 7.88 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 3.20 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge | 0.87 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge | 1.04 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow through) | 3.86 | ns |
| | RESET Low to data out Low on RD (pipelined) | 3.86 | ns |
| $t_{REMRSTB}$ | RESET removal | 1.12 | ns |
| $t_{RECRSTB}$ | RESET recovery | 5.93 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 1.18 | ns |
| $t_{CYC}$ | Clock cycle time | 10.90 | ns |
| $F_{MAX}$ | Maximum frequency | 92 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

# CS121




*Note: This is the bottom view of the package.*

## *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| CS196 | |
|---|---|
| Pin Number | AGL125 Function |
| H11 | GCB0/IO54RSB0 |
| H12 | GCA1/IO55RSB0 |
| H13 | IO49RSB0 |
| H14 | GCA2/IO57RSB0 |
| J1 | GFC2/IO115RSB1 |
| J2 | IO110RSB1 |
| J3 | IO94RSB1 |
| J4 | IO93RSB1 |
| J5 | IO89RSB1 |
| J6 | NC |
| J7 | VCC |
| J8 | VCC |
| J9 | NC |
| J10 | IO60RSB0 |
| J11 | GCB2/IO58RSB0 |
| J12 | IO50RSB0 |
| J13 | GDC1/IO61RSB0 |
| J14 | GDC0/IO62RSB0 |
| K1 | IO99RSB1 |
| K2 | GND |
| K3 | IO95RSB1 |
| K4 | VCCIB1 |
| K5 | NC |
| K6 | IO86RSB1 |
| K7 | IO80RSB1 |
| K8 | IO74RSB1 |
| K9 | IO72RSB1 |
| K10 | NC |
| K11 | VCCIB0 |
| K12 | GDA1/IO65RSB0 |
| K13 | GND |
| K14 | GDB1/IO63RSB0 |
| L1 | GEB1/IO107RSB1 |
| L2 | GEC1/IO109RSB1 |
| L3 | GEC0/IO108RSB1 |
| L4 | IO96RSB1 |

| CS196 | |
|---|---|
| Pin Number | AGL125 Function |
| L5 | IO91RSB1 |
| L6 | IO90RSB1 |
| L7 | IO83RSB1 |
| L8 | IO81RSB1 |
| L9 | IO71RSB1 |
| L10 | IO70RSB1 |
| L11 | VPUMP |
| L12 | VJTAG |
| L13 | GDA0/IO66RSB0 |
| L14 | GDB0/IO64RSB0 |
| M1 | GEB0/IO106RSB1 |
| M2 | GEA1/IO105RSB1 |
| M3 | GNDQ |
| M4 | VCCIB1 |
| M5 | IO92RSB1 |
| M6 | IO88RSB1 |
| M7 | NC |
| M8 | VCCIB1 |
| M9 | IO76RSB1 |
| M10 | GDB2/IO68RSB1 |
| M11 | VCCIB1 |
| M12 | VMV1 |
| M13 | TRST |
| M14 | VCCIB0 |
| N1 | GEA0/IO104RSB1 |
| N2 | VMV1 |
| N3 | GEC2/IO101RSB1 |
| N4 | IO100RSB1 |
| N5 | GND |
| N6 | IO87RSB1 |
| N7 | IO82RSB1 |
| N8 | IO78RSB1 |
| N9 | IO73RSB1 |
| N10 | GND |
| N11 | TCK |
| N12 | TDI |

| CS196 | |
|---|---|
| Pin Number | AGL125 Function |
| N13 | GNDQ |
| N14 | TDO |
| P1 | GND |
| P2 | GEA2/IO103RSB1 |
| P3 | FF/GEB2/IO102RSB1 |
| P4 | IO98RSB1 |
| P5 | IO97RSB1 |
| P6 | IO85RSB1 |
| P7 | IO84RSB1 |
| P8 | IO79RSB1 |
| P9 | IO77RSB1 |
| P10 | IO75RSB1 |
| P11 | GDC2/IO69RSB1 |
| P12 | GDA2/IO67RSB1 |
| P13 | TMS |
| P14 | GND |

| CS281 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| A1 | GND |
| A2 | GAB0/IO02RSB0 |
| A3 | GAC1/IO05RSB0 |
| A4 | IO13RSB0 |
| A5 | IO11RSB0 |
| A6 | IO16RSB0 |
| A7 | IO20RSB0 |
| A8 | IO24RSB0 |
| A9 | IO29RSB0 |
| A10 | VCCIB0 |
| A11 | IO39RSB0 |
| A12 | IO45RSB0 |
| A13 | IO48RSB0 |
| A14 | IO58RSB0 |
| A15 | IO61RSB0 |
| A16 | IO62RSB0 |
| A17 | GBC1/IO73RSB0 |
| A18 | GBA0/IO76RSB0 |
| A19 | GND |
| B1 | GAA2/IO225PPB3 |
| B2 | VCCIB0 |
| B3 | GAB1/IO03RSB0 |
| B4 | GAC0/IO04RSB0 |
| B5 | IO12RSB0 |
| B6 | GND |
| B7 | IO21RSB0 |
| B8 | IO26RSB0 |
| B9 | IO34RSB0 |
| B10 | IO35RSB0 |
| B11 | IO36RSB0 |
| B12 | IO46RSB0 |
| B13 | IO52RSB0 |
| B14 | GND |
| B15 | IO59RSB0 |
| B16 | GBC0/IO72RSB0 |
| B17 | GBA1/IO77RSB0 |

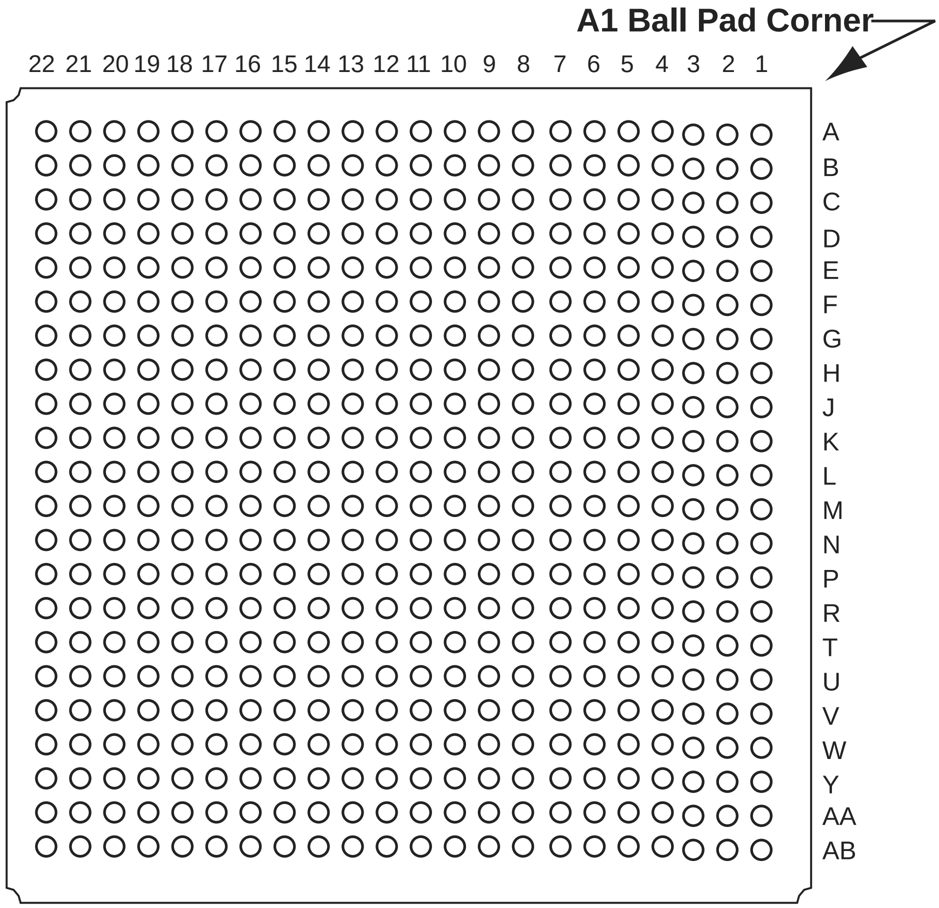
| CS281 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| B18 | VCCIB1 |
| B19 | IO79NDB1 |
| C1 | GAB2/IO224PPB3 |
| C2 | IO225NPB3 |
| C6 | IO18RSB0 |
| C14 | IO63RSB0 |
| C18 | IO78NPB1 |
| C19 | GBB2/IO79PDB1 |
| D1 | IO219PPB3 |
| D2 | IO223NPB3 |
| D4 | GAA0/IO00RSB0 |
| D5 | GAA1/IO01RSB0 |
| D6 | IO15RSB0 |
| D7 | IO19RSB0 |
| D8 | IO27RSB0 |
| D9 | IO32RSB0 |
| D10 | GND |
| D11 | IO38RSB0 |
| D12 | IO44RSB0 |
| D13 | IO47RSB0 |
| D14 | IO60RSB0 |
| D15 | GBB0/IO74RSB0 |
| D16 | GBA2/IO78PPB1 |
| D18 | GBC2/IO80PPB1 |
| D19 | IO88NPB1 |
| E1 | IO217NPB3 |
| E2 | IO221PPB3 |
| E4 | IO221NPB3 |
| E5 | IO10RSB0 |
| E6 | IO14RSB0 |
| E7 | IO25RSB0 |
| E8 | IO28RSB0 |
| E9 | IO31RSB0 |
| E10 | IO33RSB0 |
| E11 | IO42RSB0 |
| E12 | IO49RSB0 |

| CS281 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| E13 | IO53RSB0 |
| E14 | GBB1/IO75RSB0 |
| E15 | IO80NPB1 |
| E16 | IO85PPB1 |
| E18 | IO83PPB1 |
| E19 | IO84NPB1 |
| F1 | IO214NPB3 |
| F2 | GND |
| F3 | IO217PPB3 |
| F4 | IO219NPB3 |
| F5 | IO224NPB3 |
| F15 | IO85NPB1 |
| F16 | IO84PPB1 |
| F17 | IO83NPB1 |
| F18 | GND |
| F19 | IO90PPB1 |
| G1 | IO212NPB3 |
| G2 | IO211NDB3 |
| G4 | IO214PPB3 |
| G5 | IO212PPB3 |
| G7 | GAC2/IO223PPB3 |
| G8 | VCCIB0 |
| G9 | IO30RSB0 |
| G10 | IO37RSB0 |
| G11 | IO43RSB0 |
| G12 | VCCIB0 |
| G13 | IO88PPB1 |
| G15 | IO89NDB1 |
| G16 | IO89PDB1 |
| G18 | GCC0/IO91NPB1 |
| G19 | GCB1/IO92PPB1 |
| H1 | GFB0/IO208NPB3 |
| H2 | IO211PDB3 |
| H4 | GFC1/IO209PPB3 |
| H5 | GFB1/IO208PPB3 |
| H7 | VCCIB3 |

| FG144 | |
|---|---|
| Pin Number | AGL600 Function |
| K1 | GEB0/IO145NDB3 |
| K2 | GEA1/IO144PDB3 |
| K3 | GEA0/IO144NDB3 |
| K4 | GEA2/IO143RSB2 |
| K5 | IO119RSB2 |
| K6 | IO111RSB2 |
| K7 | GND |
| K8 | IO94RSB2 |
| K9 | GDC2/IO91RSB2 |
| K10 | GND |
| K11 | GDA0/IO88NDB1 |
| K12 | GDB0/IO87NDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | FF/GEB2/IO142RSB2 |
| L4 | IO136RSB2 |
| L5 | VCCIB2 |
| L6 | IO115RSB2 |
| L7 | IO103RSB2 |
| L8 | IO97RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO141RSB2 |
| M3 | IO138RSB2 |
| M4 | IO123RSB2 |
| M5 | IO126RSB2 |
| M6 | IO134RSB2 |
| M7 | IO108RSB2 |
| M8 | IO99RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG256 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| R5 | IO168RSB2 |
| R6 | IO163RSB2 |
| R7 | IO157RSB2 |
| R8 | IO149RSB2 |
| R9 | IO143RSB2 |
| R10 | IO138RSB2 |
| R11 | IO131RSB2 |
| R12 | IO125RSB2 |
| R13 | GDB2/IO115RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO183RSB2 |
| T3 | FF/GEB2/IO186RSB2 |
| T4 | IO172RSB2 |
| T5 | IO170RSB2 |
| T6 | IO164RSB2 |
| T7 | IO158RSB2 |
| T8 | IO153RSB2 |
| T9 | IO142RSB2 |
| T10 | IO135RSB2 |
| T11 | IO130RSB2 |
| T12 | GDC2/IO116RSB2 |
| T13 | IO120RSB2 |
| T14 | GDA2/IO114RSB2 |
| T15 | TMS |
| T16 | GND |

# FG484




*Note: This is the bottom view of the package.*

## *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| FG484 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| V15 | IO85RSB2 |
| V16 | GDB2/IO81RSB2 |
| V17 | TDI |
| V18 | NC |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | NC |
| W1 | NC |
| W2 | NC |
| W3 | NC |
| W4 | GND |
| W5 | IO126RSB2 |
| W6 | FF/GEB2/IO133RSB2 |
| W7 | IO124RSB2 |
| W8 | IO116RSB2 |
| W9 | IO113RSB2 |
| W10 | IO107RSB2 |
| W11 | IO105RSB2 |
| W12 | IO102RSB2 |
| W13 | IO97RSB2 |
| W14 | IO92RSB2 |
| W15 | GDC2/IO82RSB2 |
| W16 | IO86RSB2 |
| W17 | GDA2/IO80RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB3 |
| Y2 | NC |
| Y3 | NC |
| Y4 | NC |
| Y5 | GND |
| Y6 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| U1 | IO149PDB3 |
| U2 | IO149NDB3 |
| U3 | NC |
| U4 | GEB1/IO145PDB3 |
| U5 | GEB0/IO145NDB3 |
| U6 | VMV2 |
| U7 | IO138RSB2 |
| U8 | IO136RSB2 |
| U9 | IO131RSB2 |
| U10 | IO124RSB2 |
| U11 | IO119RSB2 |
| U12 | IO107RSB2 |
| U13 | IO104RSB2 |
| U14 | IO97RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO88NDB1 |
| U20 | NC |
| U21 | IO83NDB1 |
| U22 | NC |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO144PDB3 |
| V5 | GEA0/IO144NDB3 |
| V6 | IO139RSB2 |
| V7 | GEC2/IO141RSB2 |
| V8 | IO132RSB2 |
| V9 | IO127RSB2 |
| V10 | IO121RSB2 |
| V11 | IO114RSB2 |
| V12 | IO109RSB2 |
| V13 | IO105RSB2 |
| V14 | IO98RSB2 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| M3 | IO206NDB3 |
| M4 | GFA2/IO206PDB3 |
| M5 | GFA1/IO207PDB3 |
| M6 | VCCPLF |
| M7 | IO205NDB3 |
| M8 | GFB2/IO205PDB3 |
| M9 | VCC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO95PPB1 |
| M16 | GCA1/IO93PPB1 |
| M17 | GCC2/IO96PPB1 |
| M18 | IO100PPB1 |
| M19 | GCA2/IO94PPB1 |
| M20 | IO101PPB1 |
| M21 | IO99PPB1 |
| M22 | NC |
| N1 | IO201NDB3 |
| N2 | IO201PDB3 |
| N3 | NC |
| N4 | GFC2/IO204PDB3 |
| N5 | IO204NDB3 |
| N6 | IO203NDB3 |
| N7 | IO203PDB3 |
| N8 | VCCIB3 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB1 |
| N16 | IO95NPB1 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| N17 | IO100NPB1 |
| N18 | IO102NDB1 |
| N19 | IO102PDB1 |
| N20 | NC |
| N21 | IO101NPB1 |
| N22 | IO103PDB1 |
| P1 | NC |
| P2 | IO199PDB3 |
| P3 | IO199NDB3 |
| P4 | IO202NDB3 |
| P5 | IO202PDB3 |
| P6 | IO196PPB3 |
| P7 | IO193PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO112NPB1 |
| P17 | IO106NDB1 |
| P18 | IO106PDB1 |
| P19 | IO107PDB1 |
| P20 | NC |
| P21 | IO104PDB1 |
| P22 | IO103NDB1 |
| R1 | NC |
| R2 | IO197PPB3 |
| R3 | VCC |
| R4 | IO197NPB3 |
| R5 | IO196NPB3 |
| R6 | IO193NPB3 |
| R7 | GEC0/IO190NPB3 |
| R8 | VMV3 |