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"")

"	
- ,	.
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$, #	%2
,	) 3 4#
$	, , - 0! 5 0, ! 5
-	6$7 7 - . 5 - 8 8 7
9 .	))
- , #	&' : 2 ;% * &' <
-	=6! , 4
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5! , #	&: * %
> , ;> > <	&) 3> ? (' >
7 $	! 7) * &'
.	
.	) 1@$? A1@$; ! <
	,
- $	&11 B=-
, 7 -	&11 B=- ;&C* &C<
- 056	D * ' &1" C1A #1(A

Condition for V_{DD}=1.25 to 3.6V

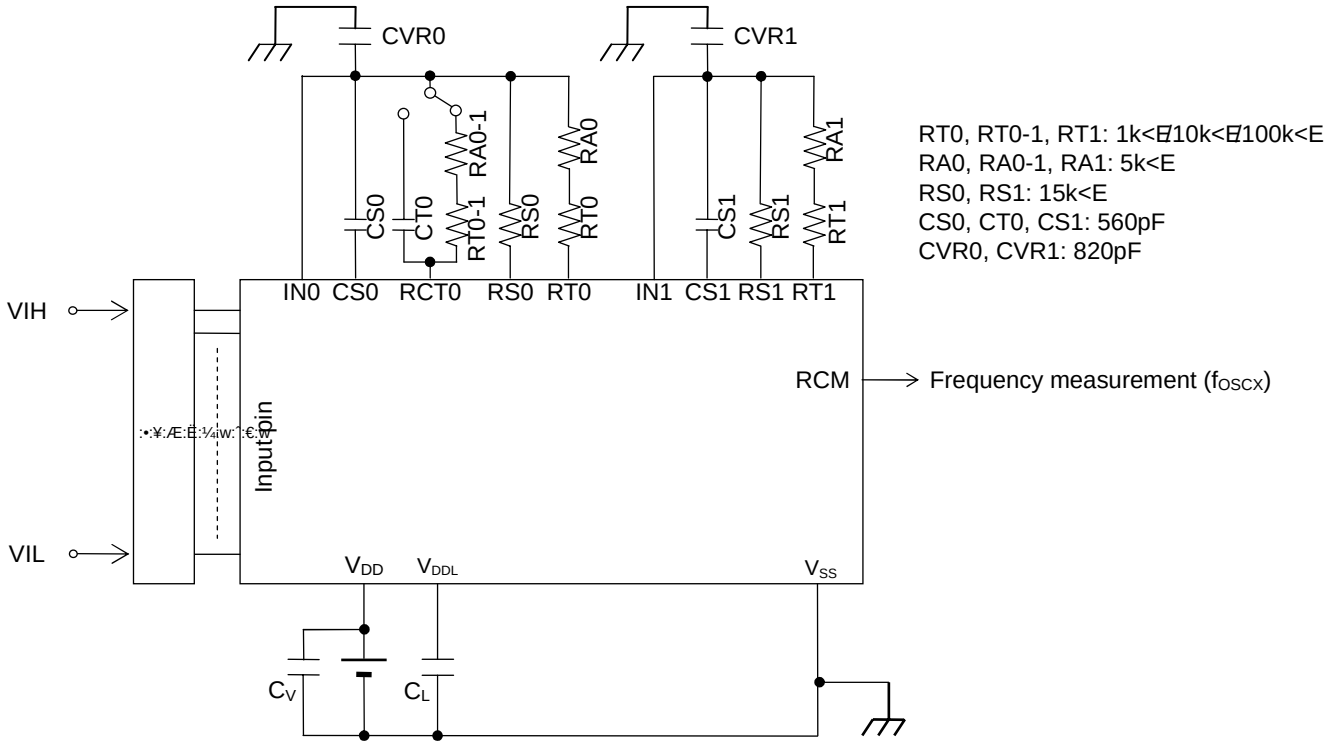
(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1 t740pF	1	Š	Š	k :
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6k :	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15k :	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105k :	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 1.5V	Kf1	RT0, RT0-1, RT1=1k :	2.139	2.381	2.632	•
	Kf2	RT0, RT0-1, RT1=10k :	0.973	1	1.028	•
	Kf3	RT0, RT0-1, RT1=100k :	0.142	0.147	0.152	•
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6k :	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15k :	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105k :	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1k :	2.227	2.432	2.626	•
	Kf2	RT0, RT0-1, RT1=10k :	0.982	1	1.018	•
	Kf3	RT0, RT0-1, RT1=100k :	0.141	0.145	0.149	•

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT0-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})}, \quad \frac{f_{OSCx}(\text{RT0-1-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})}, \quad \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor and etc.) unnecessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Package Dimensions

(Unit : mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin numb package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q409-01	Nov.7,2010	–	–	Formally edition 1
FEDL610Q409-02	Jul.12,2011	2	2	Add comment of uart half duplex communication
		3	3	Add “D” version in the supply form
FEDL610Q409-03	Jan.24,2014	All	All	Change header and footer
		2	2	Add “A” version in the supply form
		2 3	2 4	Changed the description of LCD 1/2 bias supported version
		3	4	Change from "Shipment" to " Product name – Supported Function "
		20	21	Correct minimum time of Power-on reset generated power rise time
FEDL610Q409-04	Mar.20,2014	4	4	Correct the “Product name – Supported Function”
FEDL610Q409-05	May.23,2014	-	20	Add Clock Generation Circuit Operating Conditions
		21	21	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		21	21	Correct minimum time of Power-on reset generated power rise time
		21	21	Correct the C_{GL}’s value and the C_{DL}’s value of DC CHARACTERISTICS (1/5)’s note No.2