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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	2.5MHz
Connectivity	SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.25V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q407p-nnntb03a7

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Capture
 - Time base capture \times 2 channels (4096 Hz to 32 Hz)
- PWM
 - Resolution 16 bits × 1 channel
- Synchronous serial port
 - Master/slave selectable \times 2 channel
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - Half-Duplex Communication
 - TXD/RXD \times 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- Melody driver
 - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
 - Tone length: 63 types
 - -Tempo: 15 types
 - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
 - 16-bit counter
 - Time division \times 2 channels
- General-purpose ports
 - Input-only port × 5 channels (including secondary functions)
 - Output-only port

ML610Q407: × 12 channels (including secondary functions)

- ML610Q408: × 8 channels (including secondary functions)
- ML610Q409: × 4 channels (including secondary functions)
- Input/output port \times 22 channels (including secondary functions)
- LCD driver
 - The number of segments
 - ML610Q407: 145 dots max. (29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable) ML610Q408: 165 dots max. (33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable) ML610Q409: 185 dots max. (37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable)
 - 1/1 to 1/5 duty
 - -1/2(*), 1/3 bias (built-in bias generation circuit)
 - Frame frequency selecable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
 - Bias voltage multiplying clock selectable (8 types)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
 - Programmable display allocation function
 - (*) 1/2 bias is supported by A version and D version
- Reset
 - Reset through the RESET_N pin
 - Power-on reset generation when powered on
 - Reset when oscillation stop of the low-speed clock is detected (Not supported in A version)
 - Reset by the watchdog timer (WDT) overflow



• Product name - Supported Function

/3 s //es //es //es //es //es //es //es	oscillation stop detect reset Yes Yes Yes Yes Yes Yes - -	temperature -20°C to +70°C -20°C to +70°C -20°C to +70°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -20°C to +70°C -20°C to +70°C	Product availability Yes
Yes // Ye	Yes Yes Yes Yes	-20°C to +70°C -20°C to +70°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -20°C to +70°C -20°C to +70°C	Yes Yes Yes Yes Yes Yes
Yes // Ye	Yes Yes Yes	-20°C to +70°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -20°C to +70°C -20°C to +70°C	Yes Yes Yes Yes Yes
Yes	Yes Yes	-40°C to +85°C -40°C to +85°C -40°C to +85°C -20°C to +70°C -20°C to +70°C	Yes Yes Yes Yes
Yes Yes Yes	Yes	-40°C to +85°C -40°C to +85°C -20°C to +70°C -20°C to +70°C	Yes Yes Yes
Yes Yes		-40°C to +85°C -20°C to +70°C -20°C to +70°C	Yes Yes
Yes Ves	Yes - -	-20°C to +70°C -20°C to +70°C	Yes
/es	-	-20°C to +70°C	
	-		-
/es	-		
		-20°C to +70°C	Yes
es	Yes	-20°C to +70°C	Yes
/es	Yes	-20°C to +70°C	-
Zes 🛛	Yes	-20°C to +70°C	-
/es	-	-40°C to +85°C	Yes
/es	-	-40°C to +85°C	-
/es	-	-40°C to +85°C	-
/es	Yes	-40°C to +85°C	-
7.05	Vac	-40°C to +85°C	-
05	168		
	7es 7es	7es -	Yes -40°C to +85°C Yes Yes -40°C to +85°C

-100-pin plastic	LCD	bias	Low-speed	Operating		
TQFP -	1/2	1/3	oscillation stop detect reset	temperature	Product availability	
ML610Q407-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes	
ML610Q408-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes	
ML610Q409-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes	
ML610Q407P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes	
ML610Q408P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes	
ML610Q409P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes	
ML610Q407A-xxxTB	Yes	Yes	-	-20°C to +70°C	-	
ML610Q408A-xxxTB	Yes	Yes	-	-20°C to +70°C	-	
ML610Q409A-xxxTB	Yes	Yes	-	-20°C to +70°C	-	
ML610Q407D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-	
ML610Q408D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-	
ML610Q409D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-	
ML610Q407PAxxxTB	Yes	Yes	-	-40°C to +85°C	-	
ML610Q408PAxxxTB	Yes	Yes	-	-40°C to +85°C	-	
ML610Q409PAxxxTB	Yes	Yes	-	-40°C to +85°C	-	
ML610Q407PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-	
ML610Q408PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-	
ML610Q409PDxxxTB	Yes	Yes	Yes	-40° C to $+85^{\circ}$ C	-	

xxx: ROM code number (xxx of the blank product is NNN)

Q: MTP version

P: Wide range temperature version (P version)

- A: Low-speed clock oscillation stop detection reset is disabled always and LCD 1/2 bias supported version.(A version)
- D: LCD 1/2 bias supported version (D version)

WA: Chip (Die), TB: TQFP



BLOCK DIAGRAM

ML610Q407/ML610Q408/ML610Q409 Block Diagram

Figure 1 show the block diagram of the ML610Q407/ML610Q408/ML610Q409.

"*" indicates the secondary function of each port.

"(*1)": 29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable

"(*2)": 33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable

"(*3)": 37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable

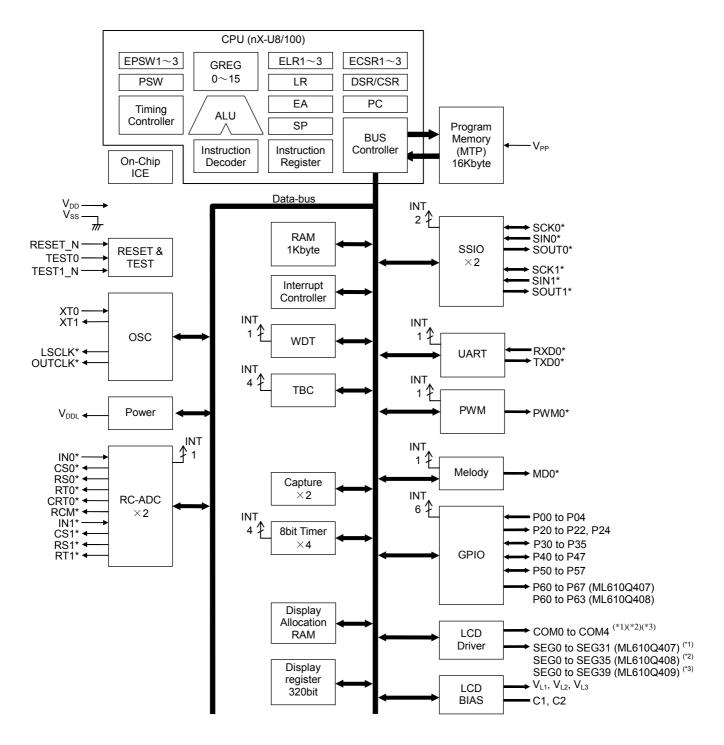
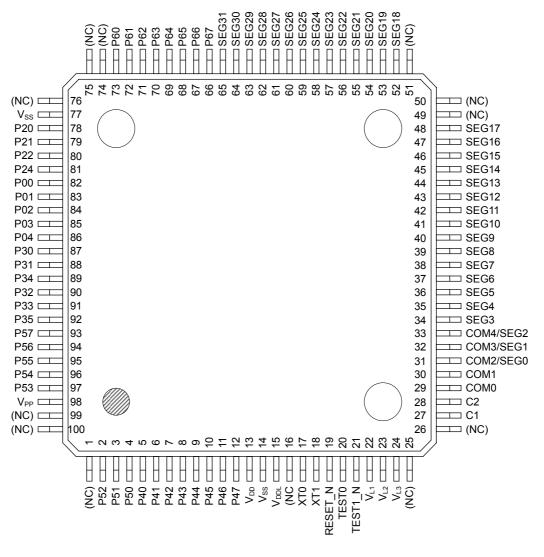


Figure 1 ML610Q407/ML610Q408/ML610Q409 Block Diagram



PIN CONFIGURATION

ML610Q407 TQFP100 Pin Layout

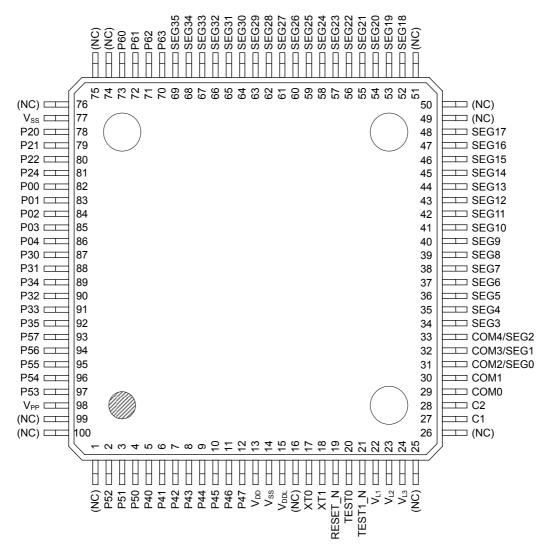


Note: The assignment of the P30 to P35 are not in order.

Figure 2 ML610Q407 TQFP100 Pin Configuration



ML610Q408 TQFP100 Pin Layout

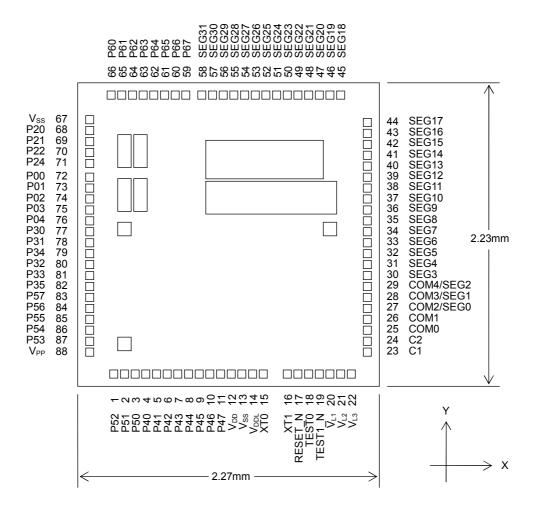


Note: The assignment of the P30 to P35 are not in order.

Figure 3 ML610Q408 TQFP100 Pin Configuration



ML610Q407 Chip Pin Layout & Dimension



Note:

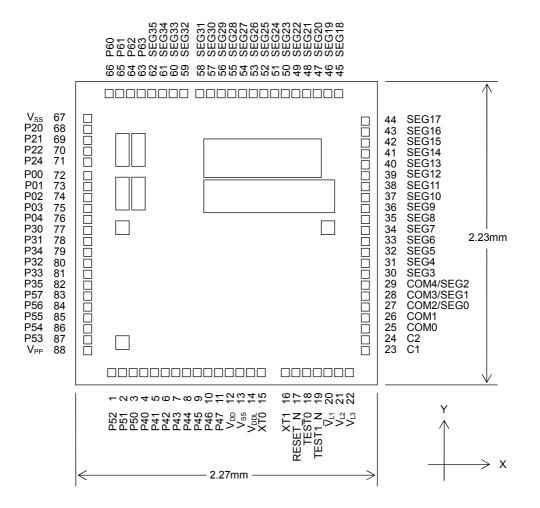
The assignment of the pads P30 to P35 are not in order.

Chip size: 2.27 mm × 2.23 mm PAD count: 88 pins Minimum PAD pitch: 80µm PAD aperture: 70µm×70µm Chip thickness: 350µm Voltage of the rear side of chip: V_{SS} level.

Figure 5 ML610Q407 Chip Layout & Dimension



ML610Q408 Chip Pin Layout & Dimension



Note: The assignment of the pads P30 to P35 are not in order.

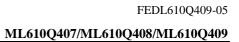
> Chip size: 2.27 mm × 2.23 mm PAD count: 88 pins Minimum PAD pitch: 80µm PAD aperture: 70µm×70µm Chip thickness: 350µm Voltage of the rear side of chip: V_{SS} level.

Figure 6 ML610Q408 Chip Layout & Dimension



PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	Ι	Crystal connection pin for low-speed clock.	_	
XT1	0	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} .		_
LSCLK	0	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	_
OUTCLK	0	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	
General-purpo	ose in	put port		
P00-P04	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpo	ose oi	utput port		
P20-P22,P24	0	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpo	ose in	put/output port		
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P57	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	0	General-purpose input/output port. These pins are for the ML610Q407/ ML610Q408, but are not provided in the ML610Q409.	Primary	Positive
P64-P67	0	General-purpose input/output port. These pins are for the ML610Q407, but are not provided in the ML610Q409.	Primary	Positive



1



Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation	type	A/D converter	. e. d.a. y	
INO		Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	_
CS0	0	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	_
RCT0	0	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	_
RS0	0	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	_
RT0	0	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	0	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	_
IN1	Ι	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	_
CS1	0	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	
RS1	0	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	_
RT1	0	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive sig	nal			
COM0-4	0	Common output pins.	—	—
SEG0-31	0	Segment output pins.	—	—
SEG32-35	0	Segment output pin. These pins are for the ML610Q408/ML610Q409, but are not provided in the ML610Q407.	—	
SEG36-39	0	Segment output pin. These pins are for the ML610Q409, but are not provided in the ML610Q407/ML610Q408.	—	
LCD driver po	wer s	upply		
V _{L1}	—	Power supply pins for LCD bias (internally generated or positive power	_	
V _{L2}	—	supply pin connected). Depending on LCD Bias setting and V_{DD} voltage	—	
V _{L3}	—	level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see user's manual.	—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is	—	
C2	—	connected between C1 and C2.		—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.		_
Power supply			,	
V _{SS}		Negative power supply pin.	_	—
V _{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	
V _{DDL}	_	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see Appendix C measuring circuit 1) is connected between this pin and V_{SS} .	_	_
V _{PP}	_	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

				$(V_{SS} = 0V)$
Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V _{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 3	V _{DDL}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 4	V _{L1}	Ta = 25°C	-0.3 to +2.0	V
Power supply voltage 5	V _{L2}	Ta = 25°C	-0.3 to +4.0	V
Power supply voltage 6	V _{L3}	Ta = 25°C	-0.3 to +6.0	V
Input voltage	V _{IN}	Ta = 25°C	–0.3 to V _{DD} +0.3	V
Output voltage	Vout	Ta = 25°C	–0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3–6, Ta = 25°C	-12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T _{STG}		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

				$(V_{SS} = 0V)$
Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	non-P version	-20 to +70	
	IOP	P version	-40 to +85	C
Operating voltage	V	f _{OP} = 30k to 625kHz	1.25 to 3.6	- v
	V _{DD}	f_{OP} = 30k to 2.5MHz	1.8 to 3.6	v
Operating frequency (CPU)	f	V _{DD} = 1.25 to 3.6V	30k to 625k	Hz
Operating frequency (CFO)	f _{OP}	V _{DD} = 1.8 to 3.6V	30k to 2.5M	ΠZ
Capacitor externally connected to V_{DDL} pin	CL		0.47±30%	μF
Capacitors externally connected to $V_{L1, 2, 3}$ pins	Ca, b, c		0.1±30%	μF
Capacitors externally connected across C1 and C2 pins	C ₁₂	_	0.47±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

 $(V_{SS} = 0V)$

Parameter	Symbol	Symbol Condition		Rating			
i didificici	Cymbol	Condition	Min.	Min. Typ.		Unit	
Low-speed crystal oscillation frequency	f _{XTL}	_	_	32.768k		Hz	
Recommended equivalent series resistance value of low-speed crystal oscillation	RL				40k	Ω	
		C _L =6pF of crystal oscillation		12			
Low-speed crystal oscillation external capacitor		C _L =9pF of crystal oscillation	_	18	18 —		
		C _L =12pF of crystal oscillation	_	24			

OPERATING CONDITIONS OF FLASH ROM

				(V _{SS} = 0V
Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	At write/erase	0 to +40	°C
	V _{DD}	At write/erase ^{*1}	2.75 to 3.6	
Operating voltage	V _{DDL}	At write/erase ^{*1}	2.5 to 2.75	V
	V _{PP}	At write/erase ^{*1}	7.7 to 8.3	
erase/program cycles	C _{EP}		80	cycles
Data retention	Y _{DR}		10	years

¹: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

DC CHARACTERISTICS (1/5)

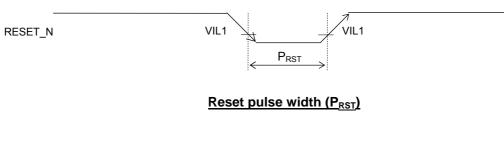
 $(V_{DD} = 1.25 \text{ to } 3.6\text{V}, V_{SS} = 0\text{V}, \text{ Ta} = -20 \text{ to } +70^{\circ}\text{C}, \text{ Ta} = -40 \text{ to } +85^{\circ}\text{C}$ for P version, unless otherwise specified)

Parameter	Symbol	Co	Condition		Rating			Measuring
Farameter	Symbol			Min.	Тур.	Max.	Unit	circuit
		V _{DD} = 1.25	Ta = 25°C	Typ. –10%	500	Typ. +10%	kHz	
500kHz/2MHz RC oscillation frequency	f _{RC}	to 3.6V	*3	Тур. –25%	500	Тур. +25%	KHZ	
	IRC	V _{DD} = 1.80 to 3.6V	Ta = 25°C	Typ. –10%	2.0	Typ. +10%	MHz	
			*3	Тур. –25%	2.0	Typ. +25%		
Low-speed crystal oscillation start time* ²	T _{XTL}	_			0.6	2	S	1
500kHz/2MHz RC oscillation start time	T _{RC}	—			_	0.3	μS	
Low-speed oscillation stop detect time ^{*1}	T _{STOP}			12	16.4	41	ms	
Reset pulse width	P _{RST}			200				
Reset noise elimination pulse width	P _{NRST}				_	0.3	μS	
Power-on reset activation power rise time	T _{POR}		_			10	ms	

*¹: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

 2 : 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF).

 $*^3$: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)





Power-on reset activation power rise time (T_{POR})



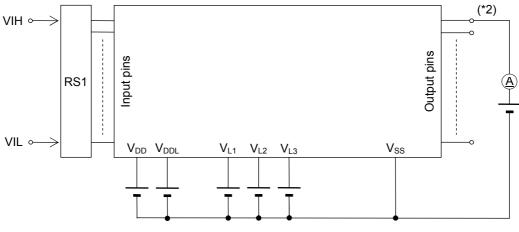
DC CHARACTERISTICS (5/5))

($(V_{DD} = 1.25 \text{ to } 3.6 \text{V}, \text{V}_{SS} = 0$	/, Ta = –20 to +70°C, Ta = –	40 to +85°C for P version, ur	less otherwise specified)

Deremeter		Condition	Rating			1 1 1	Measuring	
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit	circuit	
Input voltage 1 (RESET_N) (TEST0, TEST1_N) (P00–P04) (P30–P35) (P40–P47) (P50–P57)	VIH1	VIH1 —			V_{DD}		_	
	VIL1	V _{DD} = 1.8 to 3.6V	0		0.3 ×V _{DD}	V	5	
		V _{DD} = 1.25 to 3.6V	0		0.2 ×V _{DD}			
Input pin capacitance (P00–P04) (P30–P35) (P40–P47) (P50–P57)	CIN	f = 10kHz V _{rms} = 50mV Ta = 25°C	_		5	pF		

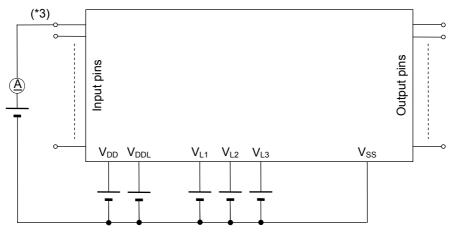


MEASURING CIRCUIT 3



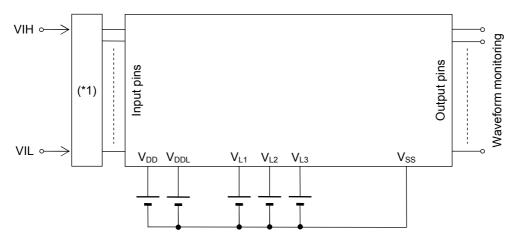
*1: Input logic circuit to determine the specified measuring conditions. *2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5



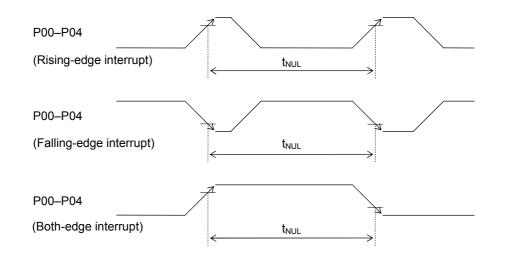
*1: Input logic circuit to determine the specified measuring conditions.



AC CHARACTERISTICS (External Interrupt)

 $(V_{DD} = 1.25 \text{ to } 3.6V, V_{SS} = 0V, Ta = -20 \text{ to } +70^{\circ}\text{C}, Ta = -40 \text{ to } +85^{\circ}\text{C}$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
	Symbol	Condition	Min.	Тур.	Max.	Unit
External interrupt disable period	T _{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8		106.8	μS

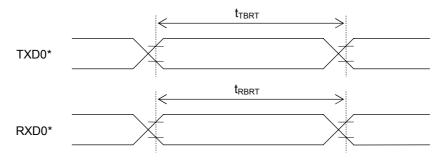


AC CHARACTERISTICS (Serial Port)

 $(V_{DD} = 1.25 \text{ to } 3.6\text{V}, V_{SS} = 0\text{V}, \text{ Ta} = -20 \text{ to } +70^{\circ}\text{C}, \text{ Ta} = -40 \text{ to } +85^{\circ}\text{C}$ for P version, unless otherwise specified)

Parameter	Symbol	Condition		Unit		
		Condition	Min.	Тур.	Max.	Unit
Transmit baud rate	t _{TBRT}			BRT* ¹		s
Receive baud rate	t _{RBRT}		BRT* ¹ _3%	BRT* ¹	BRT* ¹ +3%	S

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



*: Indicates the secondary function of the port.



AC CHARACTERISTICS (Synchronous Serial Port)

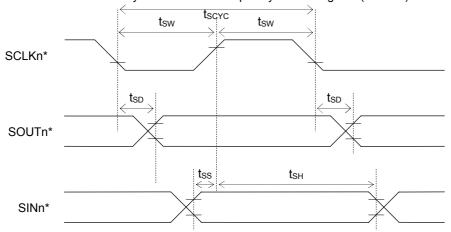
 $(V_{DD} = 1.25 \text{ to } 3.6\text{V}, V_{SS} = 0\text{V}, \text{Ta} = -20 \text{ to } +70^{\circ}\text{C}, \text{Ta} = -40 \text{ to } +85^{\circ}\text{C} \text{ for P version, unless otherwise specified})$

Parameter	Symbol	Condition	Rating				
	Symbol	Condition	Min.	Тур.	Max.	Uni	
SCLKn input cycle	+	When RC oscillation is 500kHz $*^2$ (V _{DD} = 1.25 to 3.6V)	10				
(slave mode)	tscyc	When RC oscillation is 2MHz $*^3$ (V _{DD} = 1.8 to 3.6V)	2			μs	
SCLKn output cycle (master mode)	tscyc			SCLKn*1		s	
SCLKn input pulse width		When RC oscillation is 500kHz $*^{2}$ (V _{DD} = 1.25 to 3.6V)	4 — —				
(slave mode)	t _{sw}	When RC oscillation is 2MHz $*^3$ (V _{DD} = 1.8 to 3.6V)	04			μS	
SCLKn output pulse width (master mode)	t _{sw}		SCLKn* ¹ ×0.4	SCLKn* ¹ ×0.5	SCLKn* ¹ ×0.6	s	
SOUTn output delay time (slave mode)	ter	When RC oscillation is 500kHz $*^2$ (V _{DD} = 1.25 to 3.6V) output load 10pF			500	ns	
	t _{SD}	When RC oscillation is 2MHz * ³ (V_{DD} = 1.8 to 3.6V) output load 10pF	_		240		
SOUTn output delay time (master mode)		When RC oscillation is 500kHz $*^2$ (V _{DD} = 1.25 to 3.6V) output load 10pF	_		500	ns	
	t _{SD}	When RC oscillation is 2MHz * ³ (V_{DD} = 1.8 to 3.6V) output load 10pF	_		240		
SINn input setup time (slave mode)	t _{ss}	_	80			ns	
SINn input setup time (master mode)	+	When RC oscillation is 500kHz $*^2$ (V _{DD} = 1.25 to 3.6V)	500				
	t _{ss}	When RC oscillation is 2MHz $*^3$ (V _{DD} = 1.8 to 3.6V)	240			ns	
SINn input hold time	4	When RC oscillation is 500kHz * ² (V_{DD} = 1.25 to 3.6V)	300				
	t _{sн}	When RC oscillation is 2MHz $*^3$ (V _{DD} = 1.8 to 3.6V)	80			ns	

n= 0,1

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOnMOD1) *²: When 500kHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)

*³: When 2MHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)



*: Indicates the secondary function of the port (n= 0,1)

Max.

Unit

Rating

Typ.

Min

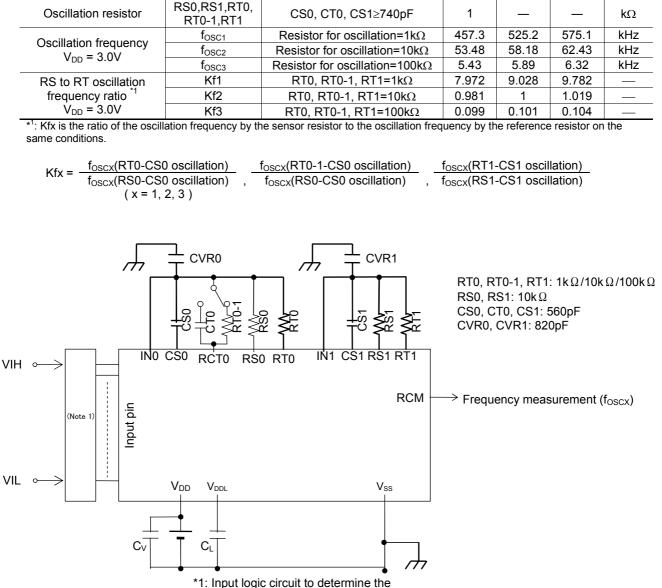


Condition for V_{DD}=1.8 to 3.6V

Parameter

AC CHARACTERISTICS (RC Oscillation A/D Converter)

Symbol



(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Condition

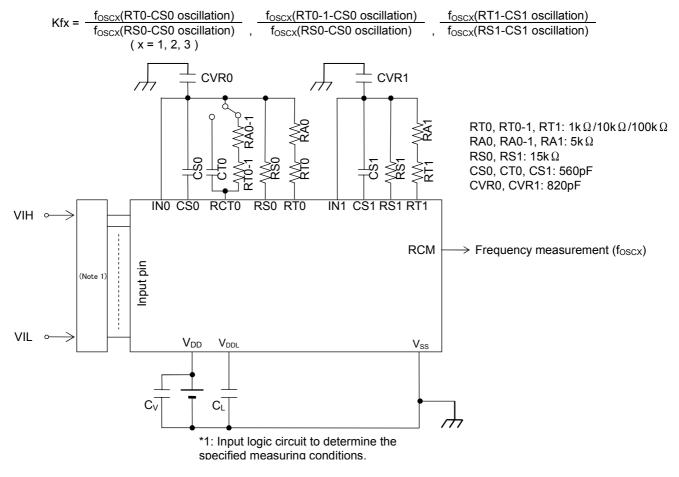
specified measuring conditions.

Condition for V_{DD}=1.25 to 3.6V

 $(\overline{V_{DD}}=1.25 \text{ to } 3.6V, V_{SS}=0V, Ta=-20 \text{ to } +70^{\circ}C, Ta=-40 \text{ to } +85^{\circ}C \text{ for P version, unless otherwise specified})$

A A A A A A A A A A A A A A A A A A A		Condition		<u> </u>			
Parameter	Symbol	Symbol Condition		Тур.	Max.	Unit	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ	
Ossillation frequency	f _{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz	
Oscillation frequency V _{DD} = 1.5V	f _{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz	
V DD - 1.0V	f _{OSC3}	Resistor for oscillation=105k Ω	5.22	5.65	6.03	kHz	
RS to RT oscillation	Kf1	RT0, RT0-1, RT1=1kΩ	2.139	2.381	2.632		
frequency ratio ^{*1} V _{DD} = 1.5V	Kf2	RT0, RT0-1, RT1=10kΩ	0.973	1	1.028		
	Kf3	RT0, RT0-1, RT1=100kΩ	0.142	0.147	0.152		
Oscillation frequency V _{DD} = 3.0V	f _{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz	
	f _{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz	
	f _{OSC3}	Resistor for oscillation=105k Ω	5.189	5.622	6.012	kHz	
RS to RT oscillation frequency ratio ^{*1}	Kf1	RT0, RT0-1, RT1=1kΩ	2.227	2.432	2.626		
	Kf2	RT0, RT0-1, RT1=10kΩ	0.982	1	1.018		
$V_{DD} = 3.0V$	Kf3	RT0, RT0-1, RT1=100k Ω	0.141	0.145	0.149		

*¹: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.



Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.

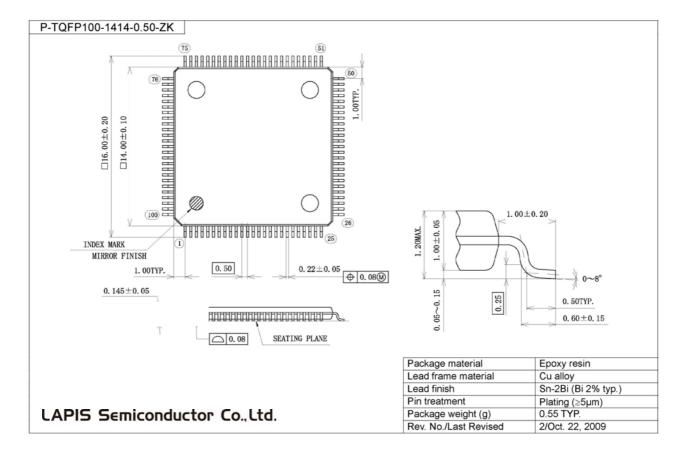
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.



FEDL610Q409-05 ML610Q407/ML610Q408/ML610Q409

Package Dimensions

(Unit:mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



Revision History

		Page				
Document No. Date	Date	Previous Edition	Current Edition	Description		
FEDL610Q409-01	Nov.7,2010	_	-	Formally edition 1		
FEDL610Q409-02 Jul.12,2011		2	2	Add comment of uart half duplex communication		
FEDL010Q409-02	Jul. 12,2011	3	3	Add "D" version in the supply form		
		All	All	Change header and footer		
		2	2	Add "A" version in the supply form		
	Jan.24,2014	2	2	Changed the description of LCD 1/2 bias supported version		
FEDL610Q409-03		3	4	Changed the description of LCD 1/2 bias supported version		
		3	4	Change from "Shipment" to " Product name – Supported Function "		
		20	21	Correct minimum time of Power-on reset generated power rise time		
FEDL610Q409-04	Mar.20,2014	4 4		Correct the "Product name – Supported Function"		
	May.23,2014	-	20	Add Clock Generation Circuit Operating Conditions		
FEDL610Q409-05		21	21	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".		
		21	21	Correct minimum time of Power-on reset generated power rise time		
		21	21	Correct the C_{GL} 's value and the C_{DL} 's value of DC CHARACTERISTICS (1/5)'s note No.2		



<u>NOTES</u>

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