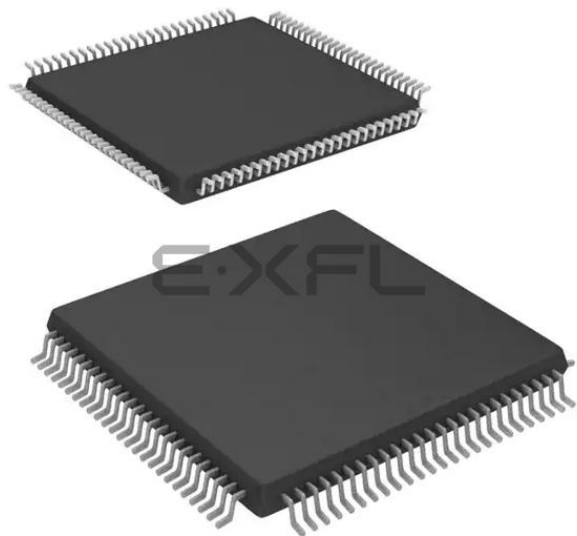




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	2.5MHz
Connectivity	SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.25V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q409-nnntbz03a7

• Product name – Supported Function

- Chip (Die) -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610Q407-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q408-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q409-xxxWA	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q407P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q408P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q409P-xxxWA	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q407A- x x x WA	Yes	Yes	-	-20°C to +70°C	Yes
ML610Q408A-xxxWA	Yes	Yes	-	-20°C to +70°C	-
ML610Q409A-xxxWA	Yes	Yes	-	-20°C to +70°C	Yes
ML610Q407D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	Yes
ML610Q408D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q409D-xxxWA	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q407PA-xxxWA	Yes	Yes	-	-40°C to +85°C	Yes
ML610Q408PA-xxxWA	Yes	Yes	-	-40°C to +85°C	-
ML610Q409PA-xxxWA	Yes	Yes	-	-40°C to +85°C	-
ML610Q407PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q408PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q409PD-xxxWA	Yes	Yes	Yes	-40°C to +85°C	-

-100-pin plastic TQFP -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610Q407-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q408-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q409-xxxTB	-	Yes	Yes	-20°C to +70°C	Yes
ML610Q407P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q408P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q409P-xxxTB	-	Yes	Yes	-40°C to +85°C	Yes
ML610Q407A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q408A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q409A-xxxTB	Yes	Yes	-	-20°C to +70°C	-
ML610Q407D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q408D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q409D-xxxTB	Yes	Yes	Yes	-20°C to +70°C	-
ML610Q407PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q408PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q409PAxxxTB	Yes	Yes	-	-40°C to +85°C	-
ML610Q407PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q408PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-
ML610Q409PDxxxTB	Yes	Yes	Yes	-40°C to +85°C	-

xxx: ROM code number (xxx of the blank product is NNN)

Q: MTP version

P: Wide range temperature version (P version)

A: Low-speed clock oscillation stop detection reset is disabled always and LCD 1/2 bias supported version.(A version)

D: LCD 1/2 bias supported version (D version)

WA: Chip (Die), TB: TQFP

BLOCK DIAGRAM

ML610Q407/ML610Q408/ML610Q409 Block Diagram

Figure 1 show the block diagram of the ML610Q407/ML610Q408/ML610Q409.

“*” indicates the secondary function of each port.

“(1)”: 29seg×5com, 30seg×4com, 31seg×3com, and 32seg×2com selectable

“(2)”: 33seg×5com, 34seg×4com, 35seg×3com, and 36seg×2com selectable

“(3)”: 37seg×5com, 38seg×4com, 39seg×3com, and 40seg×2com selectable

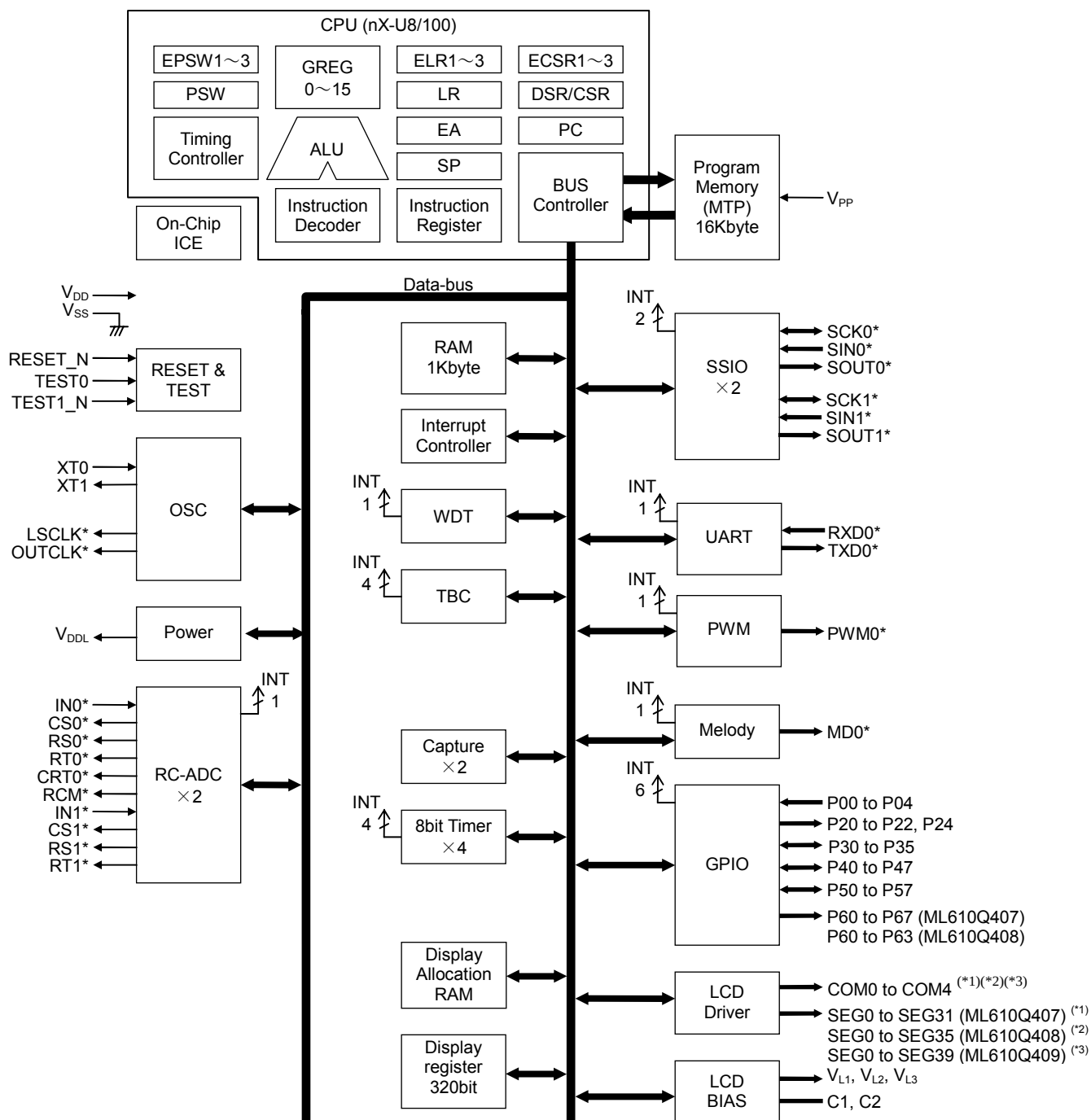


Figure 1 ML610Q407/ML610Q408/ML610Q409 Block Diagram

ML610Q407/ML610Q408/ML610Q409 Pad Coordinates
Table 1 ML610Q407/ML610Q408/ML610Q409 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610Q407/8/9	
		X (μm)	Y (μm)
1	P52	-853	-1009
2	P51	-773	-1009
3	P50	-693	-1009
4	P40	-613	-1009
5	P41	-533	-1009
6	P42	-453	-1009
7	P43	-373	-1009
8	P44	-293	-1009
9	P45	-213	-1009
10	P46	-133	-1009
11	P47	-53	-1009
12	VDD	27	-1009
13	VSS	107	-1009
14	VDDL	187	-1009
15	XT0	267	-1009
16	XT1	427	-1009
17	RESET_N	507	-1009
18	TEST0	587	-1009
19	TEST1_N	667	-1009
20	VL1	747	-1009
21	VL2	827	-1009
22	VL3	907	-1009
23	C0	1029	-840
24	C1	1029	-760
25	COM0	1029	-680
26	COM1	1029	-600
27	COM2/SEG0	1029	-520
28	COM3/SEG1	1029	-440
29	COM4/SEG2	1029	-360
30	SEG3	1029	-280
31	SEG4	1029	-200
32	SEG5	1029	-120
33	SEG6	1029	-40
34	SEG7	1029	40
35	SEG8	1029	120
36	SEG9	1029	200
37	SEG10	1029	280
38	SEG11	1029	360
39	SEG12	1029	440
40	SEG13	1029	520
41	SEG14	1029	600
42	SEG15	1029	680
43	SEG16	1029	760
44	SEG17	1029	840
45	SEG18	855	1009
46	SEG19	775	1009
47	SEG20	695	1009
48	SEG21	615	1009
49	SEG22	535	1009
50	SEG23	455	1009
51	SEG24	375	1009
52	SEG25	295	1009
53	SEG26	215	1009
54	SEG27	135	1009
55	SEG28	55	1009
56	SEG29	-25	1009
57	SEG30	-105	1009
58	SEG31	-185	1009
59	P67 ^(*)	-295	1009
	SEG32 ^(*) (*)		
60	P66 ^(*)	-375	1009
	SEG33 ^(*) (*)		
61	P65 ^(*)	-455	1009
	SEG34 ^(*) (*)		
62	P64 ^(*)	-535	1009
	SEG35 ^(*) (*)		
63	P63 ^(*) (*)	-615	1009
	SEG36 ^(*)		
64	P62 ^(*) (*)	-695	1009
	SEG37 ^(*)		
65	P61 ^(*) (*)	-775	1009
	SEG38 ^(*)		
66	P60 ^(*) (*)	-885	1009
	SEG39 ^(*)		
67	VSS	-1029	850
68	P20	-1029	770
69	P21	-1029	690
70	P22	-1029	610
71	P24	-1029	530
72	P00	-1029	430
73	P01	-1029	350
74	P02	-1029	270
75	P03	-1029	190
76	P04	-1029	110
77	P30	-1029	30
78	P31	-1029	-50
79	P34	-1029	-130
80	P32	-1029	-210
81	P33	-1029	-290
82	P35	-1029	-370
83	P57	-1029	-450
84	P56	-1029	-530
85	P55	-1029	-610
86	P54	-1029	-690
87	P53	-1029	-770
88	VPP	-1029	-850

^(*) ML610Q407 pad name, ^(*) ML610Q408 pad name, ^(*) ML610Q409 pad name

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
14,77	13,67	Vss	—	Negative power supply pin	—	—	—	—
13	12	VDD	—	Positive power supply pin	—	—	—	—
15	14	VDDL	—	Power supply pin for internal logic (internally generated)	—	—	—	—
98	88	VPP	—	Power supply pin for Flash ROM	—	—	—	—
22	20	VL1	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) ⁽²⁾	—	—	—	—
23	21	VL2	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin) ⁽²⁾	—	—	—	—
24	22	VL3	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
27	23	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
28	24	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
20	18	TEST0	I/O	Test pin	—	—	—	—
21	19	TEST1_N	I	Test pin	—	—	—	—
19	17	RESET_N	I	Reset input pin	—	—	—	—
17	15	XT0	I	Low-speed clock oscillation pin	—	—	—	—
18	16	XT1	O	Low-speed clock oscillation pin	—	—	—	—
82	72	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—
83	73	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—
84	74	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—
85	75	P03/EXI3	I	Input port, External interrupt	—	—	—	—
86	76	P04/EXI4/ T02P0CK	I	Input port, Timer 0/Timer 2/PWM0 external clock input External interrupt	—	—	—	—
78	68	P20/LED0	O	Output port	Secondary	LSCLK	O	Low-speed clock output
79	69	P21/LED1	O	Output port	Secondary	OUTCLK	O	High-speed clock output
80	70	P22/LED2	O	Output port	Secondary	MD0	O	Melody 0 output
81	71	P24/LED4	O	Output port	Secondary	PWM0	O	PWM0 output
87	77	P30	I/O	Input/output port	Secondary	IN0	I	RC type ADC0 oscillation input pin
88	78	P31	I/O	Input/output port	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
89	79	P34	I/O	Input/output port	Secondary	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
90	80	P32	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 reference resistor connection pin
91	81	P33	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 measurement resistor sensor connection pin
92	82	P35	I/O	Input/output port	Secondary	RCM	O	RC type ADC oscillation monitor

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary /Tertiary	Pin name	I/O	Function
5	4	P40	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SIN0	I	SSIO0 data input
6	5	P41	I/O	Input/output port	Secondary	—	—	—
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
7	6	P42	I/O	Input/output port	Secondary	RXD0	I	UART data input
					Tertiary	SOUT0	O	SSIO0 data output
8	7	P43	I/O	Input/output port	Secondary	TXD0	O	UART data output
					Tertiary	PWM0	O	PWM0 output
9	8	P44/ T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	Secondary	IN1	I	RC type ADC1 oscillation input pin
					Tertiary	SIN0	I	SSIO0 data input
10	9	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	Secondary	CS1	O	RC type ADC1 reference capacitor connection pin
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
11	10	P46	I/O	Input/output port	Secondary	RS1	O	RC type ADC1 reference resistor connection pin
					Tertiary	SOUT0	O	SSIO0 data output
12	11	P47	I/O	Input/output port	Secondary	RT1	O	RC type ADC1 measurement resistor sensor connection pin
4	3	P50/EXI8	I/O	Input/output port, External interrupt	Secondary	MD0	O	Melody 0 output
					Tertiary	SIN1	I	SSIO1 data input
3	2	P51/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
2	1	P52/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
97	87	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—	—
96	86	P54/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SIN1	I	SSIO1 data input
95	85	P55/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
94	84	P56/EXI8	I/O	Input/output port, External interrupt	Secondary	—	—	—
					Tertiary	SOUT1	O	SSIO1 data output
93	83	P57/EXI8	I/O	Input/output port, External interrupt	—	—	—	—

PIN No.	PAD No.	Primary function			Secondary function or Tertiary function			
		Pin name	I/O	Function	Secondary/Tertiary	Pin name	I/O	Function
29	25	COM0	O	LCD common pin	—	—	—	—
30	26	COM1	O	LCD common pin	—	—	—	—
31	27	COM2/SEG0	O	LCD common/segment pin	—	—	—	—
32	28	COM3/SEG1	O	LCD common/segment pin	—	—	—	—
33	29	COM4/SEG2	O	LCD common/segment pin	—	—	—	—
34	30	SEG3	O	LCD segment pin	—	—	—	—
35	31	SEG4	O	LCD segment pin	—	—	—	—
36	32	SEG5	O	LCD segment pin	—	—	—	—
37	33	SEG6	O	LCD segment pin	—	—	—	—
38	34	SEG7	O	LCD segment pin	—	—	—	—
39	35	SEG8	O	LCD segment pin	—	—	—	—
40	36	SEG9	O	LCD segment pin	—	—	—	—
41	37	SEG10	O	LCD segment pin	—	—	—	—
42	38	SEG11	O	LCD segment pin	—	—	—	—
43	39	SEG12	O	LCD segment pin	—	—	—	—
44	40	SEG13	O	LCD segment pin	—	—	—	—
45	41	SEG14	O	LCD segment pin	—	—	—	—
46	42	SEG15	O	LCD segment pin	—	—	—	—
47	43	SEG16	O	LCD segment pin	—	—	—	—
48	44	SEG17	O	LCD segment pin	—	—	—	—
52	45	SEG18	O	LCD segment pin	—	—	—	—
53	46	SEG19	O	LCD segment pin	—	—	—	—
54	47	SEG20	O	LCD segment pin	—	—	—	—
55	48	SEG21	O	LCD segment pin	—	—	—	—
56	49	SEG22	O	LCD segment pin	—	—	—	—
57	50	SEG23	O	LCD segment pin	—	—	—	—
58	51	SEG24	O	LCD segment pin	—	—	—	—
59	52	SEG25	O	LCD segment pin	—	—	—	—
60	53	SEG26	O	LCD segment pin	—	—	—	—
61	54	SEG27	O	LCD segment pin	—	—	—	—
62	55	SEG28	O	LCD segment pin	—	—	—	—
63	56	SEG29	O	LCD segment pin	—	—	—	—
64	57	SEG30	O	LCD segment pin	—	—	—	—
65	58	SEG31	O	LCD segment pin	—	—	—	—
66	59	P67 ^{(*)2}	O	Output port	—	—	—	—
		SEG32 ^{(*)3}	O	LCD segment pin	—	—	—	—
67	60	P66 ^{(*)2}	O	Output port	—	—	—	—
		SEG33 ^{(*)3}	O	LCD segment pin	—	—	—	—
68	61	P65 ^{(*)2}	O	Output port	—	—	—	—
		SEG34 ^{(*)3}	O	LCD segment pin	—	—	—	—
69	62	P64 ^{(*)2}	O	Output port	—	—	—	—
		SEG35 ^{(*)3}	O	LCD segment pin	—	—	—	—
70	63	P63 ^{(*)4}	O	Output port	—	—	—	—
		SEG36 ^{(*)5}	O	LCD segment pin	—	—	—	—
71	64	P62 ^{(*)4}	O	Output port	—	—	—	—
		SEG37 ^{(*)5}	O	LCD segment pin	—	—	—	—
72	65	P61 ^{(*)4}	O	Output port	—	—	—	—
		SEG38 ^{(*)5}	O	LCD segment pin	—	—	—	—
73	66	P60 ^{(*)4}	O	Output port	—	—	—	—
		SEG39 ^{(*)5}	O	LCD segment pin	—	—	—	—

(*)¹) Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see “Chapter 22 LCD Drivers. In the user’s manual”

(*)²) Pin for ML610Q407/ML610Q408.

(*)³) Pin for ML610Q409.

(*)⁴) Pin for ML610Q407.

(*)⁵) Pin for ML610Q408/ML610Q409.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V _{SS} .	—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P04	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22,P24	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P57	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P63	O	General-purpose input/output port. These pins are for the ML610Q407/ ML610Q408, but are not provided in the ML610Q409.	Primary	Positive
P64-P67	O	General-purpose input/output port. These pins are for the ML610Q407, but are not provided in the ML610Q409.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-4	O	Common output pins.	—	—
SEG0-31	O	Segment output pins.	—	—
SEG32-35	O	Segment output pin. These pins are for the ML610Q408/ML610Q409, but are not provided in the ML610Q407.	—	—
SEG36-39	O	Segment output pin. These pins are for the ML610Q409, but are not provided in the ML610Q407/ML610Q408.	—	—
LCD driver power supply				
V _{L1}	—	Power supply pins for LCD bias (internally generated or positive power supply pin connected). Depending on LCD Bias setting and V _{DD} voltage level, V _{DD} or V _{DDL} or capacitor is connected. For details of the connection method, see user's manual.	—	—
V _{L2}	—		—	—
V _{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V _{SS}	—	Negative power supply pin.	—	—
V _{DD}	—	Positive power supply pin for I/O, internal regulator, battery low detector, and power-on reset.	—	—
V _{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitor CL (see Appendix C measuring circuit 1) is connected between this pin and V _{SS} .	—	—
V _{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	−0.3 to +4.6	V
Power supply voltage 2	V _{PP}	Ta = 25°C	−0.3 to +9.5	V
Power supply voltage 3	V _{DDL}	Ta = 25°C	−0.3 to +3.6	V
Power supply voltage 4	V _{L1}	Ta = 25°C	−0.3 to +2.0	V
Power supply voltage 5	V _{L2}	Ta = 25°C	−0.3 to +4.0	V
Power supply voltage 6	V _{L3}	Ta = 25°C	−0.3 to +6.0	V
Input voltage	V _{IN}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	−0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3–6, Ta = 25°C	−12 to +11	mA
Output current 2	I _{OUT2}	Port2, Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T _{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	non-P version	−20 to +70	°C
		P version	−40 to +85	
Operating voltage	V _{DD}	f _{OP} = 30k to 625kHz	1.25 to 3.6	V
		f _{OP} = 30k to 2.5MHz	1.8 to 3.6	
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.25 to 3.6V	30k to 625k	Hz
		V _{DD} = 1.8 to 3.6V	30k to 2.5M	
Capacitor externally connected to V _{DDL} pin	C _L	—	0.47±30%	μF
Capacitors externally connected to V _{L1, 2, 3} pins	C _{a, b, c}	—	0.1±30%	μF
Capacitors externally connected across C1 and C2 pins	C ₁₂	—	0.47±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f _{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R _L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C _{DL} /C _{GL}	C _L =6pF of crystal oscillation	—	12	—	pF
		C _L =9pF of crystal oscillation	—	18	—	
		C _L =12pF of crystal oscillation	—	24	—	

DC CHARACTERISTICS (3/5)

(V_{DD} = 3.0V, V_{SS} = 0V, Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed RC500kHz/2MHz oscillation: stopped.	Ta= 25°C	—	0.4	0.8	μA
			*5	—	—	8	
Supply current 2	IDD2	CPU: In HALT state (LTBC and WDT are Operating). *3*4 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *6	Ta= 25°C	—	0.9	1.8	μA
			*5	—	—	9	
Supply current 3	IDD3	CPU: In 32.768kHz operating state. *1*3 High-speed 500kHz/2MHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	5	8	μA
			*5	—	—	15	
Supply current 4-1	IDD4-1	CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	70	100	μA
			*5	—	—	120	
Supply current 4-2	IDD4-2	CPU: In RC 2MHz operating state. LCD and BIAS circuits: Operating. *2	Ta= 25°C	—	280	350	μA
			*5	—	—	400	

*1: When the CPU operating rate is 100% (No HALT state).

*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

*3: 32.768KHz Crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)

*4: Significant bits of BLKCON0~BLKCON4 registers except DLCD bit on BLKCON4 are all "1".

*5: Recommended operating temperature (Ta = -20 to +70°C, Ta = -40 to +85°C for P version)

*6: LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC CHARACTERISTICS (4/5)

($V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20–P22,P24/ 2 nd function is selected) (P30–P36) (P40–P47) (P50–P57) (P60–P63) ^{*1 *2} (P64–P67) ^{*1}	VOH1	IOH1 = $-0.5mA$, $V_{DD} = 1.8$ to $3.6V$	V_{DD} -0.5	—	—	V	2
		IOH1 = $-0.03mA$, $V_{DD} = 1.25$ to $3.6V$	V_{DD} -0.3	—	—		
	VOL1	IOL1 = $+0.5mA$, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5		
		IOL1 = $+0.1mA$, $V_{DD} = 1.25$ to $3.6V$	—	—	0.3		
Output voltage 2 (P20–P22,P24/ 2 nd function is Not selected)	VOL2	IOL2 = $+5mA$, $V_{DD} = 1.8$ to $3.6V$	—	—	0.5		
Output voltage 3 (COM0–4) (SEG0–31) ^{*1} (SEG0–35) ^{*2} (SEG0–39) ^{*3}	VOH3	IOH4 = $-0.05mA$, $V_{L1}=1.2V$	V_{L3} -0.2	—	—		
	VOML3	IOMH4 = $+0.05mA$, $V_{L1}=1.2V$	—	—	V_{L2} $+0.2$		
	VOML3S	IOM4S = $-0.05mA$, $V_{L1}=1.2V$	V_{L2} -0.2	—	—		
	VOLM3	IOML4 = $+0.05mA$, $V_{L1}=1.2V$	—	—	V_{L1} $+0.2$		
	VOLM3S	IOML4S = $-0.05mA$, $V_{L1}=1.2V$	V_{L1} -0.2	—	—		
	VOL3	IOL4 = $+0.05mA$, $V_{L1}=1.2V$	—	—	0.2		
Output leakage (P20–P22, P24) (P30–P35) (P40–P47) (P50–P57) (P60–P63) ^{*1 *2} (P64–P67) ^{*1}	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1 = V_{DD}	0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH1 = V_{DD}	2	300	600		
	IIL2	VIL1 = V_{SS}	-1	—	—		
Input current 3 (P00–P04) (P30–P35) (P40–P47) (P50–P57)	IIH3	VIH3 = V_{DD} , $V_{DD} = 1.8$ to $3.6V$ (when pulled-down)	2	30	200		
		VIH3 = V_{DD} , $V_{DD} = 1.25$ to $3.6V$ (when pulled-down)					
	IIL3	VIL3 = V_{SS} , $V_{DD} = 1.8$ to $3.6V$ (when pulled-up)	-200	-30	-2		
		VIL3 = V_{SS} , $V_{DD} = 1.25$ to $3.6V$ (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3 = V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3 = V_{SS} (in high-impedance state)	-1	—	—		

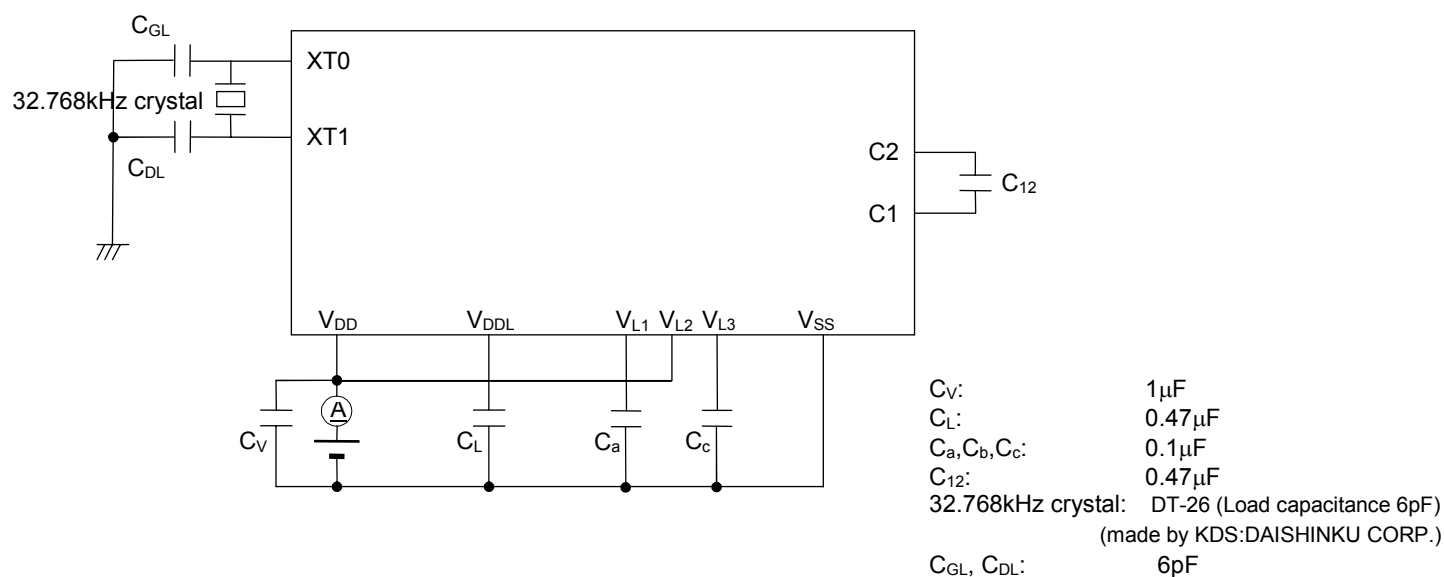
^{*1}: pins for ML610Q407

^{*2}: pins for ML610Q408

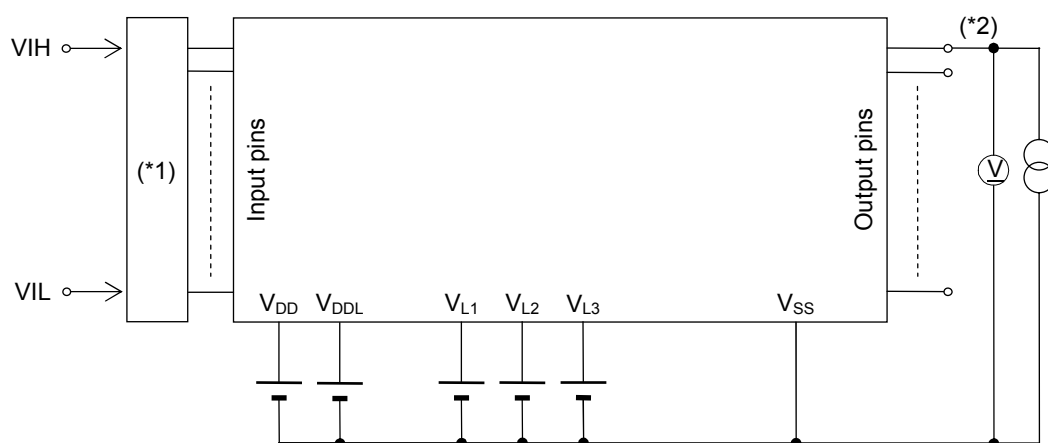
^{*3}: pins for ML610Q409

MEASURING CIRCUITS

MEASURING CIRCUIT 1



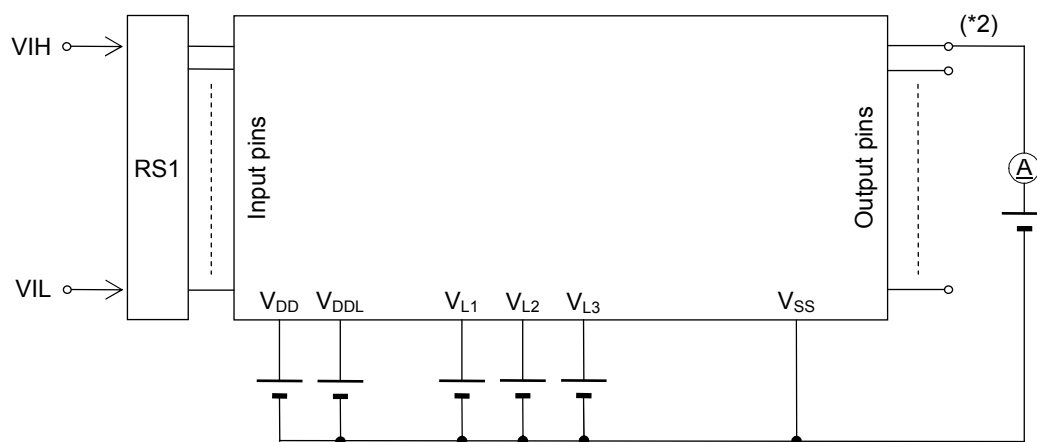
MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.

(*2) Measured at the specified output pins.

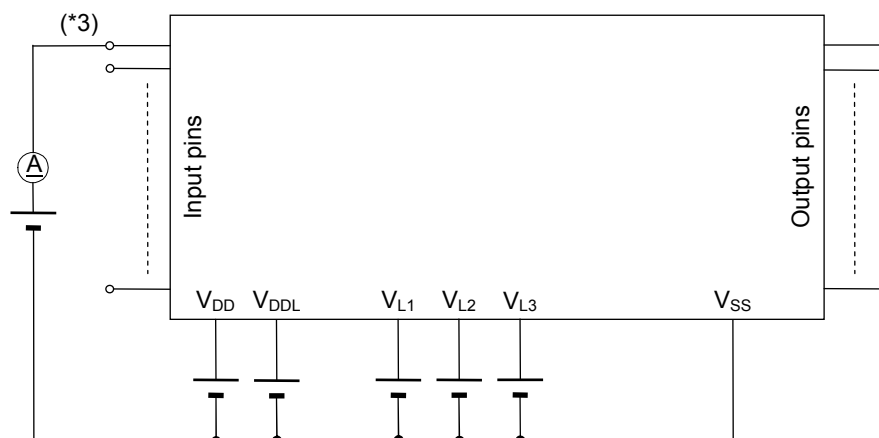
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

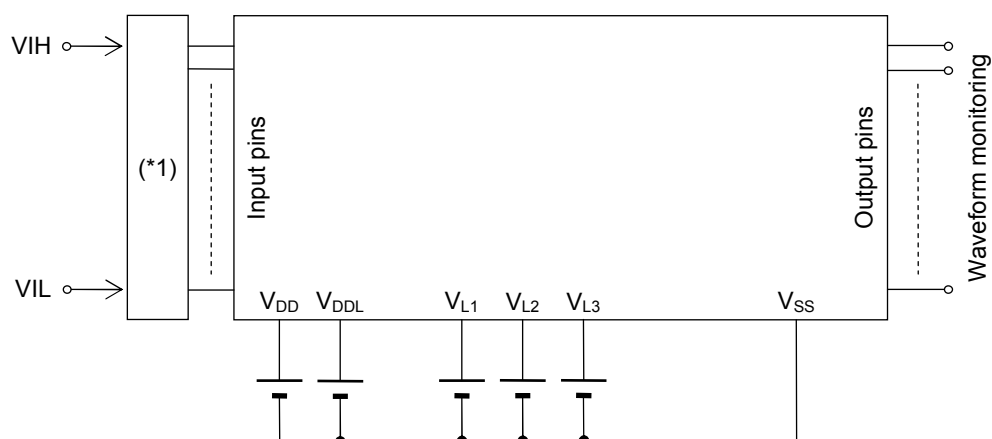
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

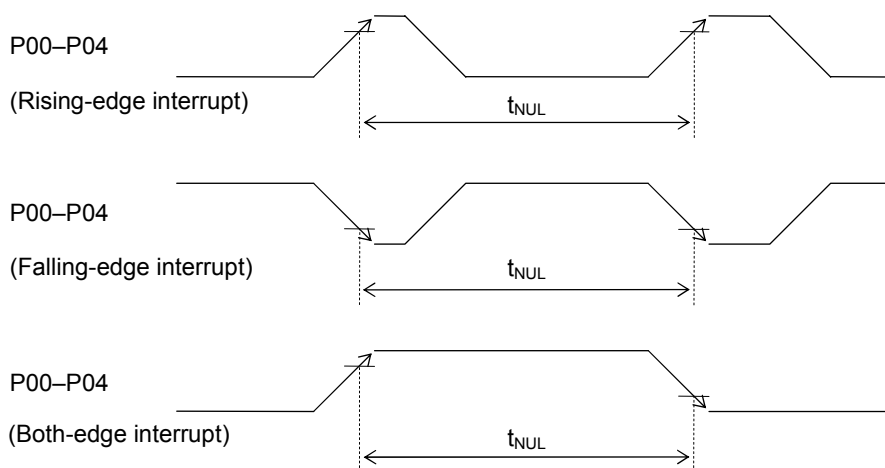


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

($V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

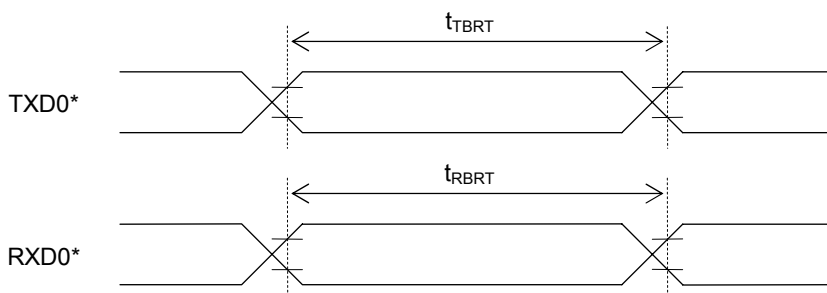


AC CHARACTERISTICS (Serial Port)

($V_{DD} = 1.25$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, $T_a = -40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT* ¹	—	s
Receive baud rate	t_{RBRT}	—	BRT* ¹ -3%	BRT* ¹	BRT* ¹ +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the serial port baud rate register (SIOBRTL,H) and the serial port mode register 0 (SIOMOD0).



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)
 $(V_{DD} = 1.25 \text{ to } 3.6\text{V}, V_{SS} = 0\text{V}, T_a = -20 \text{ to } +70^\circ\text{C}, T_a = -40 \text{ to } +85^\circ\text{C for P version, unless otherwise specified})$

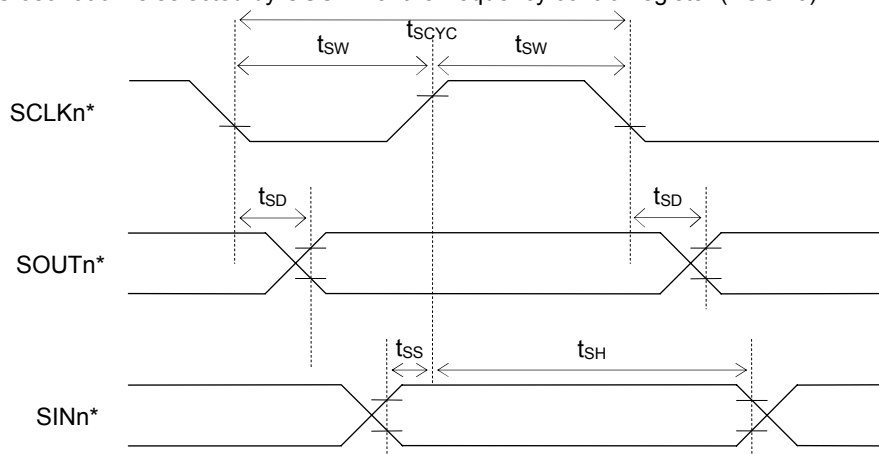
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLKn input cycle (slave mode)	t_{SCYC}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$)	10	—	—	μs
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$)	2	—	—	
SCLKn output cycle (master mode)	t_{SCYC}	—	—	SCLKn^{*1}	—	s
SCLKn input pulse width (slave mode)	t_{SW}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$)	4	—	—	μs
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$)	04	—	—	
SCLKn output pulse width (master mode)	t_{SW}	—	$\text{SCLKn}^{*1} \times 0.4$	$\text{SCLKn}^{*1} \times 0.5$	$\text{SCLKn}^{*1} \times 0.6$	s
SOUTn output delay time (slave mode)	t_{SD}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$) output load 10pF	—	—	500	ns
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$) output load 10pF	—	—	240	
SOUTn output delay time (master mode)	t_{SD}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$) output load 10pF	—	—	500	ns
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$) output load 10pF	—	—	240	
SINn input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SINn input setup time (master mode)	t_{SS}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$)	500	—	—	ns
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$)	240	—	—	
SINn input hold time	t_{SH}	When RC oscillation is 500kHz *2 ($V_{DD} = 1.25 \text{ to } 3.6\text{V}$)	300	—	—	ns
		When RC oscillation is 2MHz *3 ($V_{DD} = 1.8 \text{ to } 3.6\text{V}$)	80	—	—	

 $n = 0, 1$

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIONMOD1)

*2: When 500kHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)

*3: When 2MHz RC oscillation is selected by OSCM2 of the frequency control register (FCON0)


*: Indicates the secondary function of the port ($n = 0, 1$)

AC CHARACTERISTICS (RC Oscillation A/D Converter)

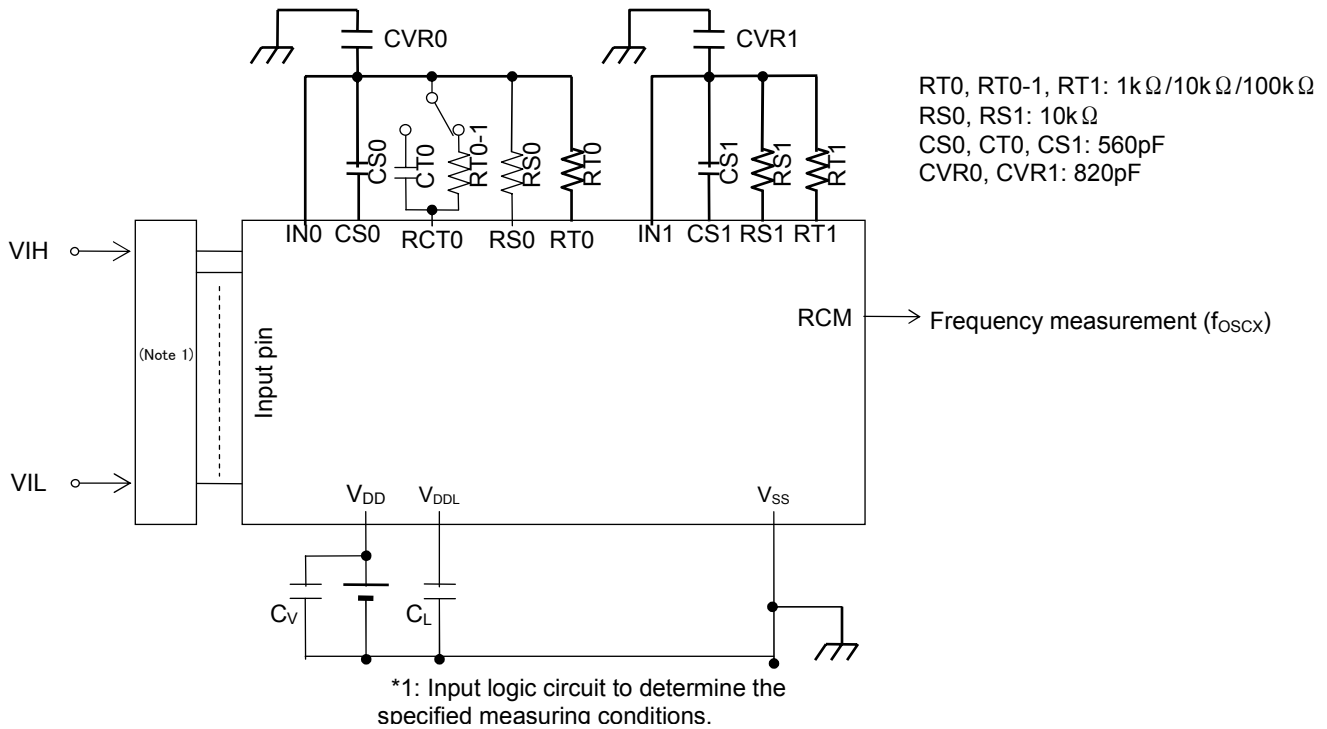
Condition for $V_{DD}=1.8$ to $3.6V$

($V_{DD}=1.8$ to $3.6V$, $V_{SS}=0V$, $T_a=-20$ to $+70^{\circ}C$, $T_a=-40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0,RT0-1,RT1	CS0, CT0, CS1 $\geq$ 740pF	1	—	—	k Ω
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=1k Ω	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10k Ω	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100k Ω	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1, RT1=1k Ω	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})} \quad (x = 1, 2, 3) , \quad \frac{f_{OSCx}(RT0-1-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})} , \quad \frac{f_{OSCx}(RT1-CS1 \text{ oscillation})}{f_{OSCx}(RS1-CS1 \text{ oscillation})}$$



Condition for $V_{DD}=1.25$ to $3.6V$

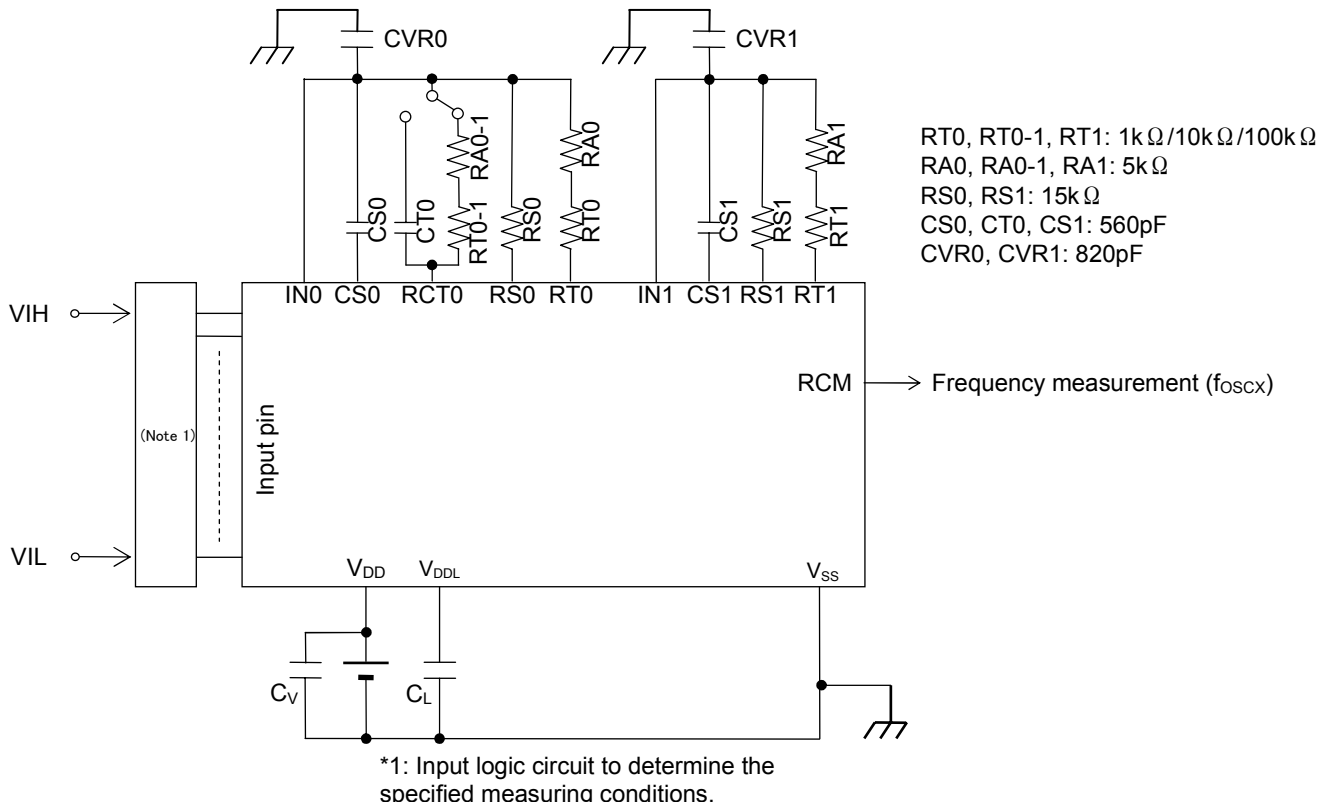
($V_{DD}=1.25$ to $3.6V$, $V_{SS}=0V$, $T_a=-20$ to $+70^{\circ}C$, $T_a=-40$ to $+85^{\circ}C$ for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0,RT0-1,RT1	CS0, CT0, CS1 $\geq 740pF$	1	—	—	k Ω
Oscillation frequency $V_{DD} = 1.5V$	f_{OSC1}	Resistor for oscillation=6k Ω	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 1.5V$	Kf1	RT0, RT0-1, RT1=1k Ω	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.142	0.147	0.152	—
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=6k Ω	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1, RT1=1k Ω	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1=10k Ω	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1=100k Ω	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \frac{f_{OSCx}(RT0-1-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \frac{f_{OSCx}(RT1-CS1 \text{ oscillation})}{f_{OSCx}(RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)

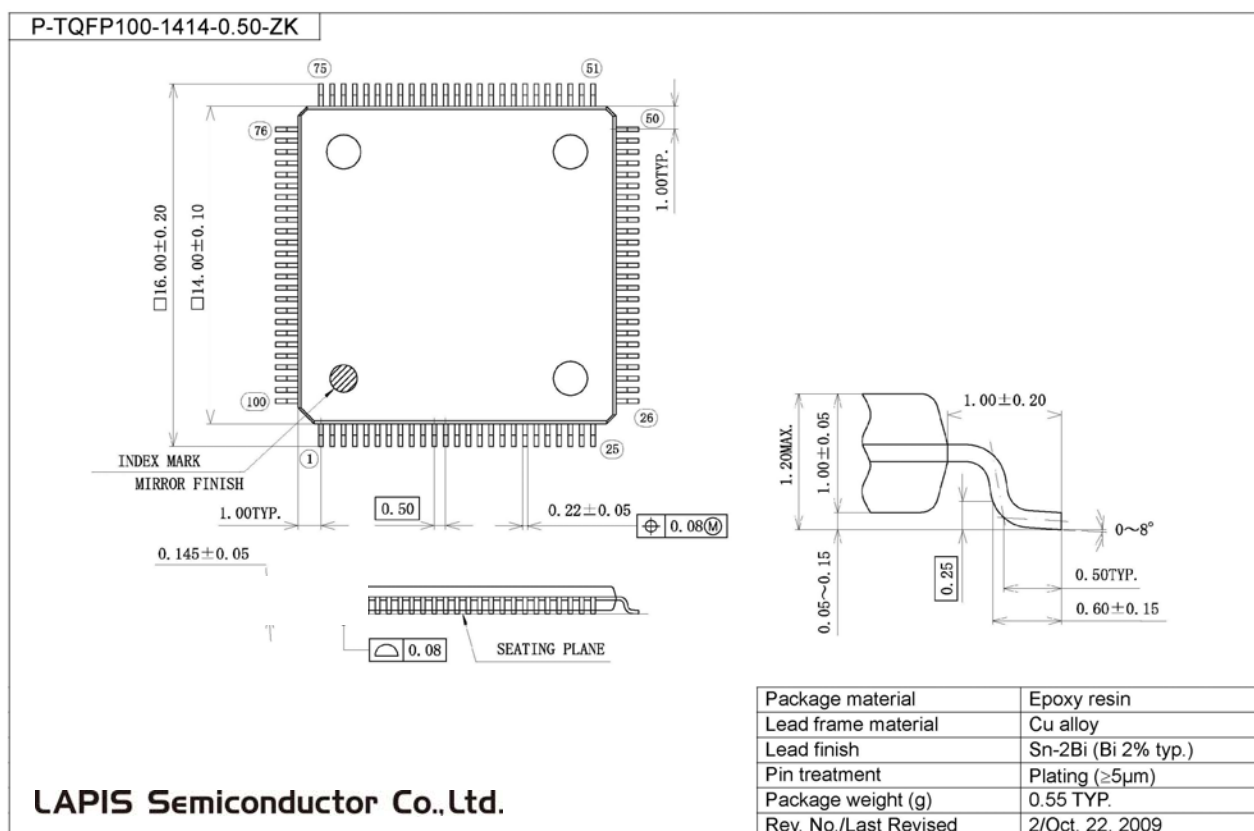


Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Package Dimensions

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q409-01	Nov.7,2010	–	–	Formally edition 1
FEDL610Q409-02	Jul.12,2011	2	2	Add comment of uart half duplex communication
		3	3	Add "D" version in the supply form
FEDL610Q409-03	Jan.24,2014	All	All	Change header and footer
		2	2	Add "A" version in the supply form
		2	2	Changed the description of LCD 1/2 bias supported version
		3	4	
		3	4	Change from "Shipment" to " Product name – Supported Function "
FEDL610Q409-04	Mar.20,2014	20	21	Correct minimum time of Power-on reset generated power rise time
		4	4	Correct the "Product name – Supported Function"
FEDL610Q409-05	May.23,2014	-	20	Add Clock Generation Circuit Operating Conditions
		21	21	Change "RESET" to " Reset pulse width (P _{RST})" and " Power-on reset activation power rise time (T _{POR})".
		21	21	Correct minimum time of Power-on reset generated power rise time
		21	21	Correct the C _{GL} 's value and the C _{DL} 's value of DC CHARACTERISTICS (1/5)'s note No.2

NOTES

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