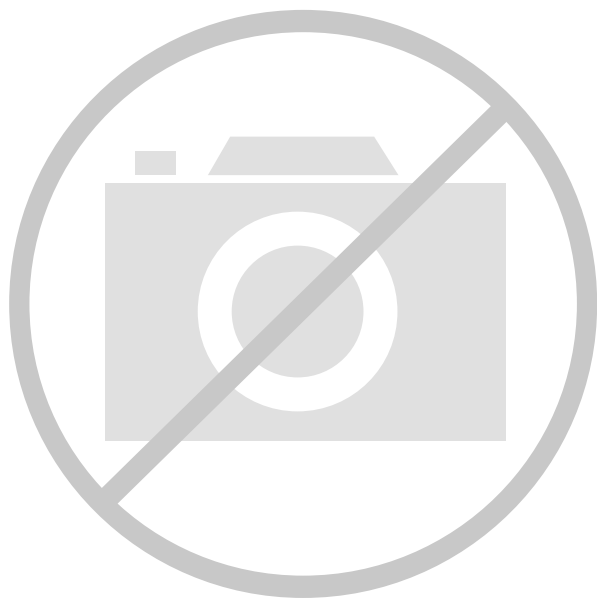




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-1ffvc1760e

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Video Codec Unit				
V _{CCINT_VCU}	Internal supply voltage for the video codec unit.	−0.500	1.000	V
PL System Monitor				
V _{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V _{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T _{STG}	Storage temperature (ambient).	−65	150	°C
T _{SOL}	Maximum soldering temperature. ⁽¹²⁾	–	260	°C
T _j	Maximum junction temperature. ⁽¹²⁾	–	125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
- AC coupled operation is not supported for RX termination = floating.
- For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
- DC coupled operation is not supported for RX termination = programmable.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
- For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 8: V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO_PSIO} + 0.30$	100%	-0.30	100%
$V_{CCO_PSIO} + 0.35$	100%	-0.35	75%
$V_{CCO_PSIO} + 0.40$	100%	-0.40	45%
$V_{CCO_PSIO} + 0.45$	100%	-0.45	40%
$V_{CCO_PSIO} + 0.50$	75%	-0.50	10%
$V_{CCO_PSIO} + 0.55$	75%	-0.55	6%
$V_{CCO_PSIO} + 0.60$	60%	-0.60	2%
$V_{CCO_PSIO} + 0.65$	30%	-0.65	0%
$V_{CCO_PSIO} + 0.70$	20%	-0.70	0%
$V_{CCO_PSIO} + 0.75$	10%	-0.75	0%
$V_{CCO_PSIO} + 0.80$	10%	-0.80	0%
$V_{CCO_PSIO} + 0.85$	8%	-0.85	0%
$V_{CCO_PSIO} + 0.90$	6%	-0.90	0%
$V_{CCO_PSIO} + 0.95$	6%	-0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V_{ICM} (V) ⁽²⁾			V_{ID} (V) ⁽³⁾		V_{OL} (V) ⁽⁴⁾	V_{OH} (V) ⁽⁵⁾	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in [Table 20](#), [Table 21](#), and [Table 22](#).
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 22: [Table 21](#) Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

Table 26: Speed Grade Designations by Device (Cont'd)

Device	Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU5EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU5EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU6CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU6EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU7CG	-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU9CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU9EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)

Table 42: Linear Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK5}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSCLK5}	Slave select asserted to next clock edge. ⁽³⁾	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS5}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO5}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK5}	Setup time, all inputs.	15 pF	2.4	–	ns
		30 pF	2.4	–	ns
T _{QSPICKD5}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPIREFCLK5}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
F _{QSPICLK5}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. T_{QSPISSCLK5} is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: ULPI Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T _{ULPIDCK}	Input setup to ULPI clock, all inputs.	4.5	–	ns
T _{ULPICKD}	Input hold to ULPI clock, all inputs.	0	–	ns
T _{ULPICKO}	ULPI clock to output valid, all outputs.	2.0	8.86	ns
F _{ULPICLK}	ULPI reference clock frequency.	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS I2C Controller Interface

Table 47: I2C Interface⁽¹⁾

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	μ s
$T_{I2CFCKH}$	SCL High time.	0.6	–	μ s
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	μ s
$T_{I2CSCKH}$	SCL High time.	4.0	–	μ s
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS DAP Interface

Table 50: DAP Interface⁽¹⁾

Symbol	Description ⁽²⁾	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time.	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time.	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay.	–	10.86	ns
$T_{PDAPCLK}$	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: UART Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate.	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate.	–	6.25	Mb/s
$F_{UART_REF_CLK}$	UART reference clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: General Purpose I/O (GPIO) Interface

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s
$T_{PWGPIOL}$	Input Low pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s

PS Trace Interface

Table 53: Trace Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle.	45	55	%
F_{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 61: PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
PLL _{REFCLK} MASK	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

- For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: PS-GTR Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T _{RTX}	TX rise time.	20%–80%	–	65	–	ps
T _{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 75: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS33_S_8	1.154	1.154	1.213	1.154	1.213	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
LVDS_25	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.164	1.223	1.164	1.223	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVTTL_F_16	1.164	1.164	1.223	1.164	1.223	2.464	2.464	2.732	2.464	2.732	1.750	1.750	1.986	1.750	1.986	ns
LVTTL_F_4	1.164	1.164	1.223	1.164	1.223	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVTTL_F_8	1.164	1.164	1.223	1.164	1.223	2.582	2.582	2.787	2.582	2.787	1.910	1.910	2.063	1.910	2.063	ns
LVTTL_S_12	1.164	1.164	1.223	1.164	1.223	2.731	2.731	3.075	2.731	3.075	2.072	2.072	2.343	2.072	2.343	ns
LVTTL_S_16	1.164	1.164	1.223	1.164	1.223	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVTTL_S_4	1.164	1.164	1.223	1.164	1.223	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns
LVTTL_S_8	1.164	1.164	1.223	1.164	1.223	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
SLVS_400_25	1.020	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.780	0.867	0.780	0.867	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
SSTL12_S	0.780	0.780	0.867	0.780	0.867	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
SSTL135_F	0.798	0.798	0.881	0.798	0.881	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
SSTL135_II_F	0.798	0.798	0.881	0.798	0.881	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
SSTL135_II_S	0.798	0.798	0.881	0.798	0.881	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
SSTL135_S	0.798	0.798	0.881	0.798	0.881	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
SSTL15_F	0.838	0.838	0.880	0.838	0.880	1.612	1.612	1.754	1.612	1.754	1.357	1.357	1.464	1.357	1.464	ns
SSTL15_II_F	0.838	0.838	0.880	0.838	0.880	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
SSTL15_II_S	0.838	0.838	0.880	0.838	0.880	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
SSTL15_S	0.838	0.838	0.880	0.838	0.880	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
SSTL18_II_F	0.947	0.947	1.021	0.947	1.021	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
SSTL18_II_S	0.947	0.947	1.021	0.947	1.021	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
SSTL18_I_F	0.947	0.947	1.021	0.947	1.021	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
SSTL18_I_S	0.947	0.947	1.021	0.947	1.021	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
SUB_LVDS	1.002	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS18_F_8	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.600	0.573	0.600	0.733	0.733	0.767	0.733	0.767	ns
LVC MOS18_M_12	0.418	0.418	0.445	0.418	0.445	0.640	0.640	0.678	0.640	0.678	0.670	0.670	0.709	0.670	0.709	ns
LVC MOS18_M_2	0.418	0.418	0.445	0.418	0.445	0.798	0.798	0.822	0.798	0.822	0.991	0.991	1.016	0.991	1.016	ns
LVC MOS18_M_4	0.418	0.418	0.445	0.418	0.445	0.664	0.664	0.693	0.664	0.693	0.798	0.798	0.836	0.798	0.836	ns
LVC MOS18_M_6	0.418	0.418	0.445	0.418	0.445	0.629	0.629	0.663	0.629	0.663	0.735	0.735	0.775	0.735	0.775	ns
LVC MOS18_M_8	0.418	0.418	0.445	0.418	0.445	0.626	0.626	0.661	0.626	0.661	0.705	0.705	0.746	0.705	0.746	ns
LVC MOS18_S_12	0.418	0.418	0.445	0.418	0.445	0.795	0.795	0.861	0.795	0.861	0.683	0.683	0.721	0.683	0.721	ns
LVC MOS18_S_2	0.418	0.418	0.445	0.418	0.445	0.862	0.862	0.897	0.862	0.897	1.076	1.076	1.098	1.076	1.098	ns
LVC MOS18_S_4	0.418	0.418	0.445	0.418	0.445	0.716	0.716	0.758	0.716	0.758	0.829	0.829	0.872	0.829	0.872	ns
LVC MOS18_S_6	0.418	0.418	0.445	0.418	0.445	0.682	0.682	0.724	0.682	0.724	0.724	0.724	0.762	0.724	0.762	ns
LVC MOS18_S_8	0.418	0.418	0.445	0.418	0.445	0.707	0.707	0.760	0.707	0.760	0.709	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.462	0.426	0.426	0.443	0.426	0.443	0.548	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.462	0.553	0.553	0.582	0.553	0.582	0.645	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.462	0.749	0.749	0.803	0.749	0.803	0.821	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.447	0.441	0.441	0.459	0.441	0.459	0.560	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.447	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.447	0.760	0.760	0.818	0.760	0.818	0.837	0.837	0.899	0.837	0.899	ns
LVDS	0.539	0.539	0.620	0.539	0.620	0.626	0.626	0.662	0.626	0.662	960.447	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.415	0.502	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	8.792	0.914	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.407	0.430	0.407	0.430	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.407	0.430	0.407	0.430	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.407	0.430	0.407	0.430	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.409	0.431	0.409	0.431	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.431	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.431	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.409	0.431	0.409	0.431	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.409	0.431	0.409	0.431	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.409	0.431	0.409	0.431	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.399	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.399	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.399	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, LVDCI, HSLVDCI, 1.5V	LVC MOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVC MOS, LVDCI, HSLVDCI, 1.8V	LVC MOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	$V_{REF} - 0.2875$	$V_{REF} + 0.2875$	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
POD10, 1.0V	POD10	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.7
POD12, 1.2V	POD12	$V_{REF} - 0.24$	$V_{REF} + 0.24$	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	$0.75 - 0.325$	$0.75 + 0.325$	0 ⁽⁶⁾	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	$0.9 - 0.4$	$0.9 + 0.4$	0 ⁽⁶⁾	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	$0.675 - 0.2875$	$0.675 + 0.2875$	0 ⁽⁶⁾	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	$0.75 - 0.325$	$0.75 + 0.325$	0 ⁽⁶⁾	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.4$	$0.9 + 0.4$	0 ⁽⁶⁾	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.5 - 0.2$	$0.5 + 0.2$	0 ⁽⁶⁾	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	$0.9 - 0.125$	$0.9 + 0.125$	0 ⁽⁶⁾	–
LVDS_25, 2.5V	LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁶⁾	–

PLL Switching Characteristics

Table 86: PLL Specification⁽¹⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F _{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3					
PLL_T _{OUTDUTY}	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100					μs
PLL_F _{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. ⁽⁵⁾	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_F _{BANDWIDTH}	PLL bandwidth at typical.	14	14	14	14	14	MHz
PLL_F _{DPCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

[Table 94](#) summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 94: GTH Transceiver DC Specifications

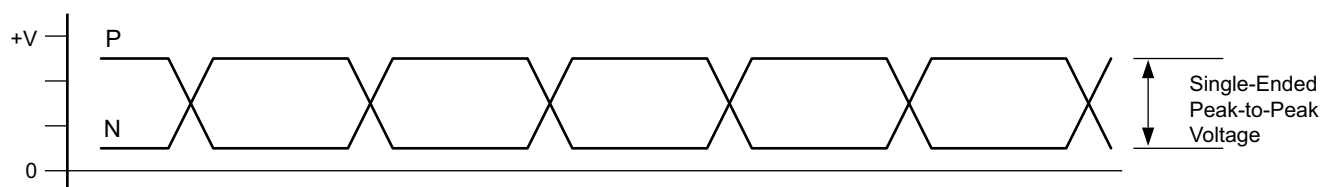
Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage.	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽³⁾		–	100	–	nF

Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
- V_{RX_TERM} is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.

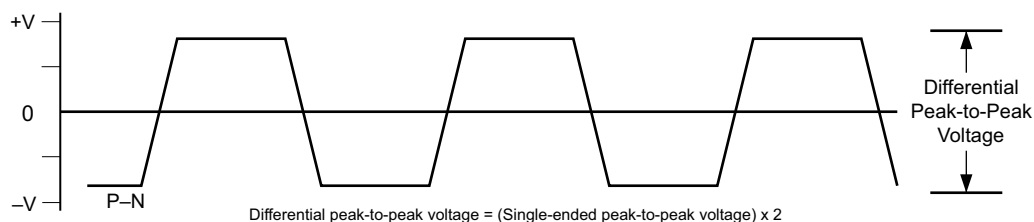
Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI



X16653-101316

Figure 5: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 6: Differential Peak-to-Peak Voltage

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 107: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 109: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F _{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYCRANGE}	CPLL line rate range ⁽¹⁾	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE1}	QPLL0 line rate range ⁽²⁾	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE2}	QPLL1 line rate range ⁽³⁾	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL0_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 113: GTY Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock.		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10 ⁶	UI

Table 114: GTY Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Table 116: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s	0.25	–	–	UI	
J _{T_SJ28.21}	Sinusoidal jitter (QPLL) ⁽³⁾	28.21 Gb/s	0.30	–	–	UI	
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI	
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI	
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾							
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI	
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI	
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI	
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI	

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale+ Interlaken](#). The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 118](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 119](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 120](#)).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See [Table 109](#) for the F_{GTYMAX} description.

Table 118: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	
F _{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F _{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 119: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V			0.72V					
		-3 ⁽¹⁾	-2 ⁽¹⁾	-1	-2	-1						
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	250.00	N/A	MHz					
		Min ⁽²⁾	Max	Min ⁽²⁾	Max	Min	Max	Min ⁽²⁾	Max	Min	Max	
F _{CORE_CLK}	Interlaken core clock	412.50 ⁽³⁾	479.20	412.50 ⁽³⁾	479.20	N/A	412.50	429.69	N/A	MHz		
F _{LBUS_CLK}	Interlaken local bus clock	300.00 ⁽⁴⁾	349.52	300.00 ⁽⁴⁾	349.52	N/A	300.00	349.52	N/A	MHz		

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F _{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F _{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz