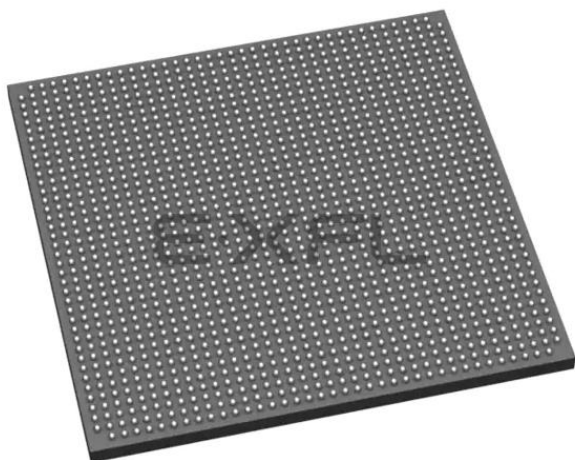




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-1ffvf1517e

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO} + 0.30$	100%	-0.30	100%
$V_{CCO} + 0.35$	100%	-0.35	90%
$V_{CCO} + 0.40$	100%	-0.40	78%
$V_{CCO} + 0.45$	100%	-0.45	40%
$V_{CCO} + 0.50$	100%	-0.50	24%
$V_{CCO} + 0.55$	100%	-0.55	18.0%
$V_{CCO} + 0.60$	100%	-0.60	13.0%
$V_{CCO} + 0.65$	100%	-0.65	10.8%
$V_{CCO} + 0.70$	92%	-0.70	9.0%
$V_{CCO} + 0.75$	92%	-0.75	7.0%
$V_{CCO} + 0.80$	92%	-0.80	6.0%
$V_{CCO} + 0.85$	92%	-0.85	5.0%
$V_{CCO} + 0.90$	92%	-0.90	4.0%
$V_{CCO} + 0.95$	92%	-0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO} + 0.30$	100%	-0.30	100%
$V_{CCO} + 0.35$	100%	-0.35	100%
$V_{CCO} + 0.40$	92%	-0.40	92%
$V_{CCO} + 0.45$	50%	-0.45	50%
$V_{CCO} + 0.50$	20%	-0.50	20%
$V_{CCO} + 0.55$	10%	-0.55	10%
$V_{CCO} + 0.60$	6%	-0.60	6%
$V_{CCO} + 0.65$	2%	-0.65	2%
$V_{CCO} + 0.70$	2%	-0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μs .

Table 9: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (Cont'd)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current.	XCZU2	N/A	26	26	26	26	mA
		XCZU3	N/A	26	26	26	26	mA
		XCZU4	32	32	32	32	32	mA
		XCZU5	32	32	32	32	32	mA
		XCZU6	33	33	33	33	33	mA
		XCZU7	56	56	56	56	56	mA
		XCZU9	33	33	33	33	33	mA
		XCZU11	56	56	56	56	56	mA
		XCZU15	33	33	33	33	33	mA
		XCZU17	74	74	74	74	74	mA
		XCZU19	74	74	74	74	74	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current.	XCZU2	N/A	6	6	6	6	mA
		XCZU3	N/A	6	6	6	6	mA
		XCZU4	9	9	9	9	9	mA
		XCZU5	9	9	9	9	9	mA
		XCZU6	25	24	24	24	24	mA
		XCZU7	16	15	15	15	15	mA
		XCZU9	25	24	24	24	24	mA
		XCZU11	23	22	22	22	22	mA
		XCZU15	29	28	28	28	28	mA
		XCZU17	37	35	35	35	35	mA
		XCZU19	37	35	35	35	35	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Table 15: SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	5.8	−5.8
HSTL_I_12	−0.300	V _{REF} − 0.080	V _{REF} + 0.080	V _{CCO} + 0.300	25% V _{CCO}	75% V _{CCO}	4.1	−4.1
HSTL_I_18	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	6.2	−6.2
HSUL_12	−0.300	V _{REF} − 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.1	−0.1
LVC MOS12	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	Note 4	Note 4
LVC MOS15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVC MOS18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVDCI_15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
LVDCI_18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
SSTL12	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	8.0	−8.0
SSTL135	−0.300	V _{REF} − 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	9.0	−9.0
SSTL15	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.175	V _{CCO} /2 + 0.175	10.0	−10.0
SSTL18_I	−0.300	V _{REF} − 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 − 0.470	V _{CCO} /2 + 0.470	7.0	−7.0
MIPI_DPHY_DCI_LP ⁽⁶⁾	−0.300	0.550	0.880	V _{CCO} + 0.300	0.050	1.100	0.01	−0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 16](#), [Table 20](#), [Table 21](#), and [Table 22](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: DC Input Levels for Single-ended POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V _{IL}		V _{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300
POD12	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 17: Differential SelectIO DC Input and Output Levels

I/O Standard	V _{ICM} (V) ⁽¹⁾			V _{ID} (V) ⁽²⁾			V _{ILHS} ⁽³⁾	V _{IHHS} ⁽³⁾	V _{OCM} (V) ⁽⁴⁾			V _{OD} (V) ⁽⁵⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS ⁽⁸⁾	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS ⁽⁹⁾	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage (Q – $\bar{Q}$).
- V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage (Q – $\bar{Q}$).
- LVDS_25 is specified in Table 23.
- LVDS is specified in Table 24.
- Only the SUB_LVDS receiver is supported in HD I/O banks.
- High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 18: Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks

I/O Standard	V _{ICM} (V) ⁽¹⁾			V _{ID} (V) ⁽²⁾		V _{OL} (V) ⁽³⁾	V _{OH} (V) ⁽⁴⁾	I _{OL}	I _{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V _{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V _{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V _{CCO}	80% V _{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V _{CCO} /2) – 0.470	(V _{CCO} /2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V _{CCO} /2) – 0.600	(V _{CCO} /2) + 0.600	13.4	–13.4

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage.
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V_{ICM} (V) ⁽²⁾			V_{ID} (V) ⁽³⁾		V_{OL} (V) ⁽⁴⁾	V_{OH} (V) ⁽⁵⁾	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: Table 21 Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 25](#).

Table 25: Speed Specification Version By Device

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: Generic Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK1}	Quad-SPI clock duty cycle.	15 pF	45	55	%
T _{QSPISSCLK1}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
T _{QSPISCLKSS1}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
T _{QSPICKO1}	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
T _{QSPIDCK1}	Setup time, all inputs.	15 pF	0.9	–	ns
T _{QSPICKD1}	Hold time, all inputs.	15 pF	1.0	–	ns
F _{QSPICLK1}	Quad-SPI device clock frequency.	15 pF	–	150	MHz
F _{QSPIREFCLK1}	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK2}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSCLK2}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS2}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO2}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK2}	Setup time, all inputs.	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
T _{QSPICKD2}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPICLK2}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
F _{QSPIREFCLK2}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3 (1)	-2 (1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF_DELAY_PAD_I}}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF_DELAY_O_PAD}}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I / O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Block RAM and FIFO Switching Characteristics

Table 80: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F _{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T _{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Table 102: GTH Transceiver User Clock Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{TXIN2}	TXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F _{RXIN2}	RXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

- Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).

Table 103: GTH Transceiver Transmitter Switching Characteristics

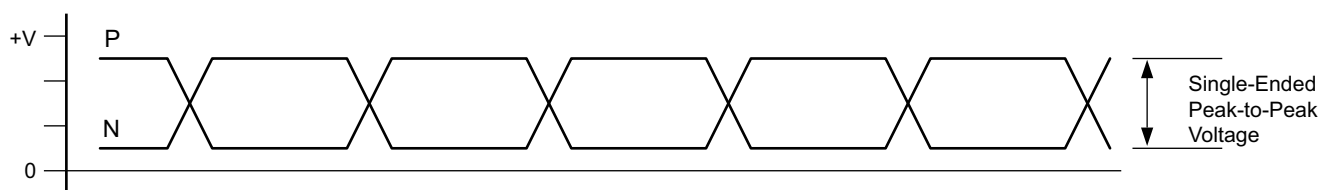
Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 105: GTH Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽¹⁾	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽²⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽²⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI ⁽²⁾	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort ⁽²⁾	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PH-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

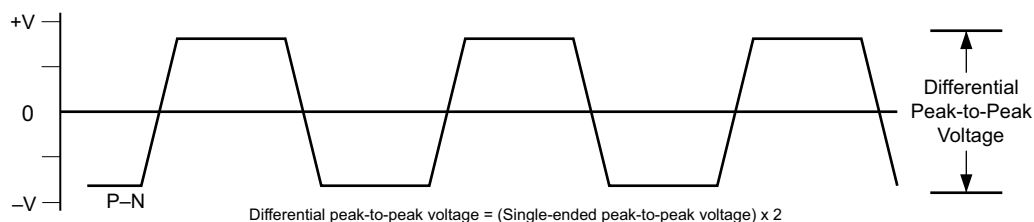
Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.



X16653-101316

Figure 5: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 6: Differential Peak-to-Peak Voltage

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 107: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

Table 113: GTY Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock.		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10 ⁶	UI

Table 114: GTY Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 117](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽²⁾	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽³⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽³⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale+ Interlaken](#). The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 118](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 119](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 120](#)).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See [Table 109](#) for the F_{GTYMAX} description.

Table 118: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	
F _{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F _{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 119: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V			0.72V					
		-3 ⁽¹⁾	-2 ⁽¹⁾	-1	-2	-1						
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	250.00	N/A	MHz					
		Min ⁽²⁾	Max	Min ⁽²⁾	Max	Min	Max	Min ⁽²⁾	Max	Min	Max	
F _{CORE_CLK}	Interlaken core clock	412.50 ⁽³⁾	479.20	412.50 ⁽³⁾	479.20	N/A	412.50	429.69	N/A	MHz		
F _{LBUS_CLK}	Interlaken local bus clock	300.00 ⁽⁴⁾	349.52	300.00 ⁽⁴⁾	349.52	N/A	300.00	349.52	N/A	MHz		

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F _{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F _{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

PL SYSMON I2C/PMBus Interfaces

Table 125: PL SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 126: PL SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Configuration Switching Characteristics

Table 127: Configuration Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T _{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T _{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
T _{PS_PROG_B}	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F _{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F _{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
F _{CFGMCLK}	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
F _{CFGMCLKTOL}	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T _{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max