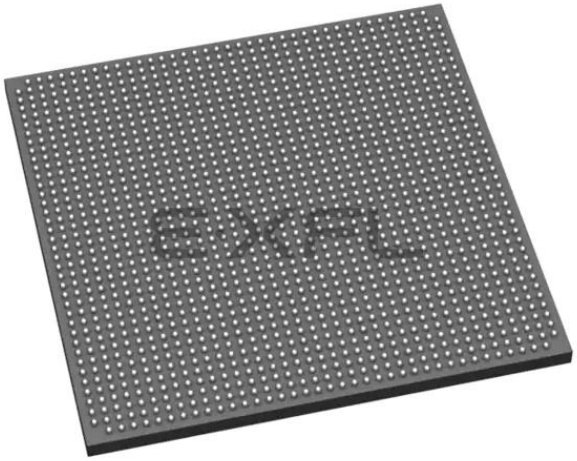

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-1ffvf1517i

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
PL System Monitor					
V_{CCADC}	PL System Monitor supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j(13)	Junction temperature operating range for extended (E) temperature devices.(14)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. $V_{CC\_PSINTFP\_DDR}$ must be tied to $V_{CC\_PSINTFP}$.
4. Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at ±5% and 1.1V +0.07V/–0.04V depending upon the tolerances required by specific memory standards.
5. Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at ±5%.
6. If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX}. The V_{CC_PSAUX} maximum of 1.89V is acceptable on an unused V_{CC_PSBATT}.
7. V_{CCINT_IO} must be connected to V_{CCBRAM}.
8. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
9. V_{CCAUX_IO} must be connected to V_{CCAUX}.
10. The lower absolute voltage specification always applies.
11. A total of 200 mA per bank should not be exceeded.
12. Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
13. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 69 and Table 124) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
14. Devices labeled with the speed/temperature grade of -2LE normally operate under Extended (E) temperature grade specifications with a maximum junction temperature of 100°C. However, E temperature grade devices can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do at 100°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
I_{CC_PSBATT}(4)(5)	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC enabled.	–	–	3650	nA
	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC disabled.	–	–	650	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC enabled.	–	–	3150	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC disabled.	–	–	150	nA
I_{PSFS}(6)	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in HP I/O banks(8) (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%(7)	120	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%(7)	240	+10%(7)	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks(1)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 11: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels(1)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:
1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels(1)**

DDR Standard	V_{IL}		V_{IH}		V_{OL}(2)	V_{OH}(2)	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:
1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 23: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	100	350	600(2)	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 24: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF}(2)	Differential output voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}(2)	Output common-mode voltage.	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}(3)	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600(3)	mV
V_{ICM_DC}(4)	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC}(5)	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

PS Configuration

Table 39: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: **Boundary-Scan Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: **Generic Quad-SPI Interface(1)**

Symbol	Description	Load Conditions(2)	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
$T_{QSPISSSCLK1}$	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
$T_{QSPISCLKSS1}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
$T_{QSPICKO1}$	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
$T_{QSPIDCK1}$	Setup time, all inputs.	15 pF	0.9	–	ns
$T_{QSPICKD1}$	Hold time, all inputs.	15 pF	1.0	–	ns
$F_{QSPICLK1}$	Quad-SPI device clock frequency.	15 pF	–	150	MHz
$F_{QSPIREFCLK1}$	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK2}$	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS2}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO2}$	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK2}$	Setup time, all inputs.	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
$T_{QSPICKD2}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPICLK2}$	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
$F_{QSPIREFCLK2}$	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.

PS Gigabit Ethernet Controller Interface

Table 44: **RGMII Interface(1)**

Symbol	Description	Min	Max	Units
$T_{DCGEMTXCLK}$	Transmit clock duty cycle.	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time.	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time.	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time.	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period.	400	–	ns
$T_{MDIOCKL}$	MDC low time.	160	–	ns
$T_{MDIOCKH}$	MDC high time.	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time.	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time.	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time.	–1.0	15	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency.	–	125	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency.	–	125	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: **SD/SDIO Interface(1)**

Symbol	Description	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
$T_{DCDDRCLK}$	SD device clock duty cycle.	45	55	%
$T_{SDDDRCKO1}$	Clock to output delay, data.(2)	1.0	6.8	ns
$T_{SDDRIVW}$	Input valid data window.(3)	3.5	–	ns
$T_{SDDDRDCK2}$	Input setup time, command.	4.7	–	ns
$T_{SDDDRCKD2}$	Input hold time, command.	1.5	–	ns
$T_{SDDDRCKO2}$	Clock to output delay, command.	1.0	13.8	ns
$F_{SDDDRCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface SDR104				
$T_{DCSDHSCLK1}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO1}$	Clock to output delay, all outputs.(2)	1.0	3.2	ns
$T_{SDSDR1IVW}$	Input valid data window.(3)	0.5	–	UI
$F_{SDSDRCLK1}$	SDR104 mode device clock frequency.	–	200	MHz
SD/SDIO Interface SDR50/25				
$T_{DCSDHSCLK2}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO2}$	Clock to output delay, all outputs.(2)	1.0	6.8	ns
$T_{SDSDR2IVW}$	Input valid data window.(3)	0.3	–	UI

Table 60: **PS-GTR Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequencies supported.	PCI Express	100 MHz			
		SATA	125 MHz or 150 MHz			
		USB 3.0	26 MHz, 52 MHz, or 100 MHz			
		DisplayPort	27 MHz, 108 MHz, or 135 MHz			
		SGMII	125 MHz			
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only.	40	–	60	%
		USB 3.0 with reference clock <40 MHz.	47.5	–	52.5	%

Table 63: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX_{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: **PCI Express Protocol Characteristics (PS-GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:
1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: **DisplayPort Protocol Characteristics (PS-GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:
1. Only the transmitter is supported.

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 22. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3(3)		-2(3)		-1		-2(3)		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(4)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(4)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0 (6)	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0 (6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0 (6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0 (6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0 (6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0 (6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 (6)	–
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
$T_{PSMMCMCC\_ZU2}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU2}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU3}$		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU3}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU4}$		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU4}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU5}$		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU5}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU6}$		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU6}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU7}$		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
$T_{PHMMCMCC\_ZU7}$		Hold		–0.14	–0.14	–0.14	0.37	0.38	ns
$T_{PSMMCMCC\_ZU9}$		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU9}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU11}$		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
$T_{PHMMCMCC\_ZU11}$		Hold		–0.08	–0.08	0.04	0.35	0.74	ns
$T_{PSMMCMCC\_ZU15}$		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU15}$		Hold		–0.10	–0.10	–0.10	0.17	0.19	ns
$T_{PSMMCMCC\_ZU17}$		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU17}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns
$T_{PSMMCMCC\_ZU19}$		Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU19}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

Table 94 summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 94: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage.	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.(1)	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor.(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

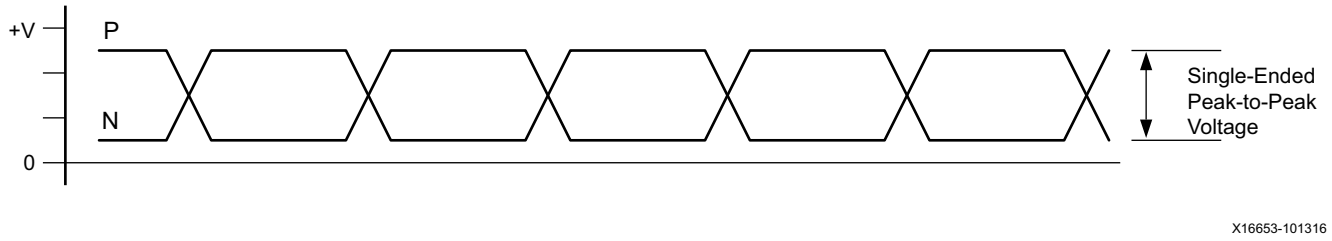

Figure 5: **Single-Ended Peak-to-Peak Voltage**

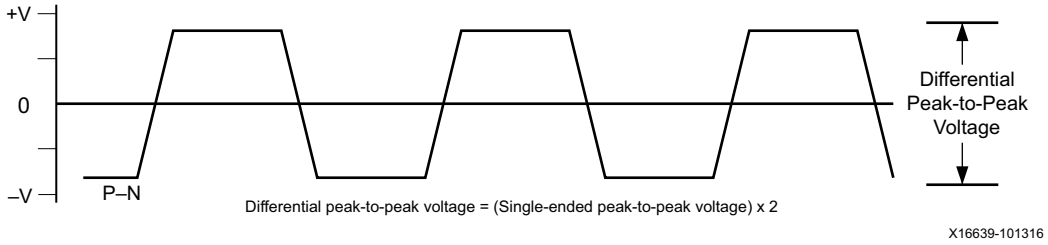

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 117. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(2)	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(3)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(3)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale+ Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 121: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2(1)	-1	-2	-1(2)	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:
1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V_{CCINT}=0.72V.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include this block.

Table 122: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:
1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.