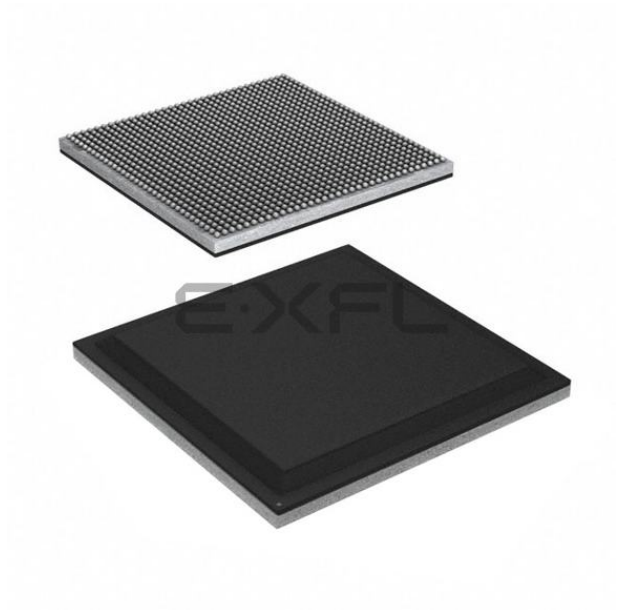

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-2ffvc1156e

Table 1: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	–0.500	2.000	V
V_{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V_{PSIN}[2]	PS I/O input voltage.	–0.500	V_{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V_{CCO_PSDDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage.	–0.500	1.000	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	–0.500	2.000	V
V_{CCAUX_IO}[4]	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V_{REF}	Input reference voltage.	–0.500	2.000	V
V_{IN}[2][5][7]	I/O input voltage for HD I/O banks.[6]	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	–0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad.	–20	20	mA
I_{RMS}	Available RMS output current at the pad.	–20	20	mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.[8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.[9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–	6	mA

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
I_{CC_PSBATT}(4)(5)	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC enabled.	–	–	3650	nA
	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC disabled.	–	–	650	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC enabled.	–	–	3150	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC disabled.	–	–	150	nA
I_{PSFS}(6)	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in HP I/O banks(8) (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%(7)	120	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%(7)	240	+10%(7)	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **PS MIO Pull-up and Pull-down Current**

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 3.3V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 2.5V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 1.8V.	15	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	15	65	µA

PL I/O Levels

Table 14: **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Table 31: **PS NAND NV-DDR Synchronous Performance**

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
NV-DDR(1)	5	200	200	200	Mb/s
	4	166.6	166.6	166.6	Mb/s
	3	133.3	133.3	133.3	Mb/s
	2	100	100	100	Mb/s
	1	66.6	66.6	66.6	Mb/s
	0	40	40	40	Mb/s

Notes:
1. The PS NAND memory controller interface for NV-DDR switching characteristics meets the requirements of the ONFI 3.1 specification.

Table 32: **PS NAND SDR Asynchronous Performance**

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
SDR(1)(2)	5	50	50	50	Mb/s
	4	40	40	40	Mb/s
	3	33.3	33.3	33.3	Mb/s
	2	28.5	28.5	28.5	Mb/s
	1	20	20	20	Mb/s
	0	10	10	10	Mb/s

Notes:
1. The PS NAND memory controller interface for SDR switching characteristics meets the requirements of the ONFI 3.1 specification.
2. The NAND controller reference clock frequency maximum is 83 MHz.

Table 33: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency.	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency.	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency.	–	25	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency.	–	125	MHz
$F_{FCIDMACLK}$	Flow control interface DMA maximum frequency.	–	333	MHz
F_{AXICLK}	Maximum AXI interface performance.	–	333	MHz
$F_{DPLIVEVIDEO}$	DisplayPort controller live video interface maximum frequency.	–	300	MHz

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

PS Gigabit Ethernet Controller Interface

Table 44: **RGMII Interface(1)**

Symbol	Description	Min	Max	Units
$T_{DCGEMTXCLK}$	Transmit clock duty cycle.	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time.	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time.	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time.	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period.	400	–	ns
$T_{MDIOCKL}$	MDC low time.	160	–	ns
$T_{MDIOCKH}$	MDC high time.	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time.	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time.	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time.	–1.0	15	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency.	–	125	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency.	–	125	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: **SD/SDIO Interface(1)**

Symbol	Description	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
$T_{DCDDRCLK}$	SD device clock duty cycle.	45	55	%
$T_{SDDDRCKO1}$	Clock to output delay, data.(2)	1.0	6.8	ns
$T_{SDDRIVW}$	Input valid data window.(3)	3.5	–	ns
$T_{SDDDRDCK2}$	Input setup time, command.	4.7	–	ns
$T_{SDDDRCKD2}$	Input hold time, command.	1.5	–	ns
$T_{SDDDRCKO2}$	Clock to output delay, command.	1.0	13.8	ns
$F_{SDDDRCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface SDR104				
$T_{DCSDHSCLK1}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO1}$	Clock to output delay, all outputs.(2)	1.0	3.2	ns
$T_{SDSDR1IVW}$	Input valid data window.(3)	0.5	–	UI
$F_{SDSDRCLK1}$	SDR104 mode device clock frequency.	–	200	MHz
SD/SDIO Interface SDR50/25				
$T_{DCSDHSCLK2}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO2}$	Clock to output delay, all outputs.(2)	1.0	6.8	ns
$T_{SDSDR2IVW}$	Input valid data window.(3)	0.3	–	UI

PS I2C Controller Interface

Table 47: **I2C Interface(1)**

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µs
$T_{I2CSCKH}$	SCL High time.	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple-timer Counter Interface

Table 54: **Triple-timer Counter Interface**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	–	16.5	MHz
$T_{TTCICLKL}$	Triple-timer counter input clock high pulse width.	1.5 x $1/F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$T_{TTCICLKH}$	Triple-timer counter input clock low pulse width.	1.5 x $1/F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	–	$F_{LPD\_LSBUS\_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: **Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS33_S_8	1.154	1.154	1.213	1.154	1.213	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
LVDS_25	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.164	1.223	1.164	1.223	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVTTL_F_16	1.164	1.164	1.223	1.164	1.223	2.464	2.464	2.732	2.464	2.732	1.750	1.750	1.986	1.750	1.986	ns
LVTTL_F_4	1.164	1.164	1.223	1.164	1.223	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVTTL_F_8	1.164	1.164	1.223	1.164	1.223	2.582	2.582	2.787	2.582	2.787	1.910	1.910	2.063	1.910	2.063	ns
LVTTL_S_12	1.164	1.164	1.223	1.164	1.223	2.731	2.731	3.075	2.731	3.075	2.072	2.072	2.343	2.072	2.343	ns
LVTTL_S_16	1.164	1.164	1.223	1.164	1.223	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVTTL_S_4	1.164	1.164	1.223	1.164	1.223	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns
LVTTL_S_8	1.164	1.164	1.223	1.164	1.223	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
SLVS_400_25	1.020	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.780	0.867	0.780	0.867	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
SSTL12_S	0.780	0.780	0.867	0.780	0.867	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
SSTL135_F	0.798	0.798	0.881	0.798	0.881	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
SSTL135_II_F	0.798	0.798	0.881	0.798	0.881	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
SSTL135_II_S	0.798	0.798	0.881	0.798	0.881	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
SSTL135_S	0.798	0.798	0.881	0.798	0.881	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
SSTL15_F	0.838	0.838	0.880	0.838	0.880	1.612	1.612	1.754	1.612	1.754	1.357	1.357	1.464	1.357	1.464	ns
SSTL15_II_F	0.838	0.838	0.880	0.838	0.880	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
SSTL15_II_S	0.838	0.838	0.880	0.838	0.880	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
SSTL15_S	0.838	0.838	0.880	0.838	0.880	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
SSTL18_II_F	0.947	0.947	1.021	0.947	1.021	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
SSTL18_II_S	0.947	0.947	1.021	0.947	1.021	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
SSTL18_I_F	0.947	0.947	1.021	0.947	1.021	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
SSTL18_I_S	0.947	0.947	1.021	0.947	1.021	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
SUB_LVDS	1.002	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

IOB High Performance (HP) Switching Characteristics

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

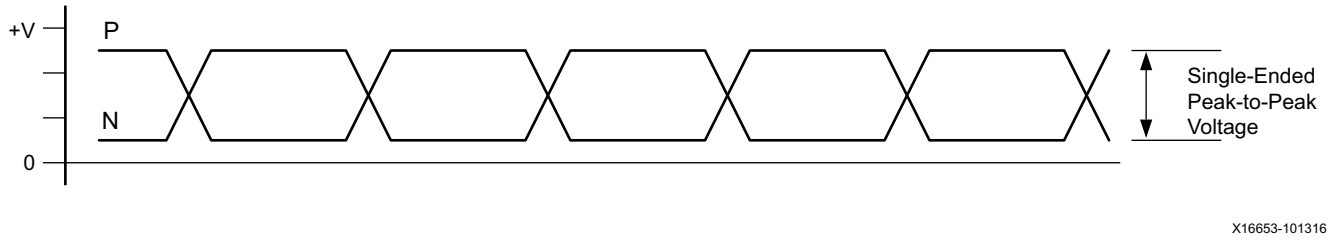

Figure 3: **Single-Ended Peak-to-Peak Voltage**

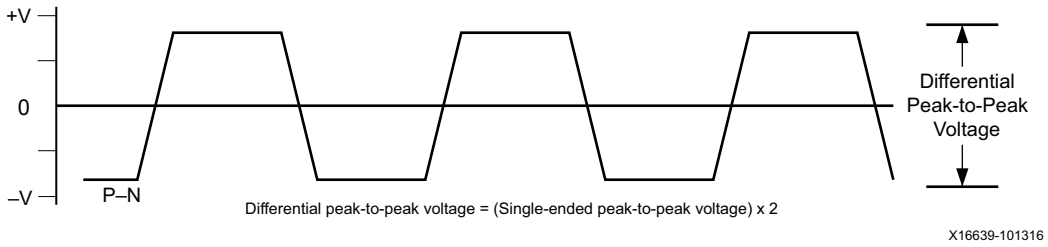

Figure 4: **Differential Peak-to-Peak Voltage**

Table 95 and Table 96 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 95: **GTH Transceiver Clock Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 96: **GTH Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N.	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N.	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage. (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage.	R_T = 100Ω across P and N signals	300	–	500	mV

Table 102: **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 105: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(1)	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(2)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(2)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI(2)	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort(2)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:
1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Table 113: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 114: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)(5)	-2(3)	-1(5)	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Video Codec Performance

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 123: **VCU Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 124: **PL SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity(2)	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic (T_j = –55°C to 125°C)	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Configuration Switching Characteristics

Table 127: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T_{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T_{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
$T_{PS\_PROG\_B}$	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max