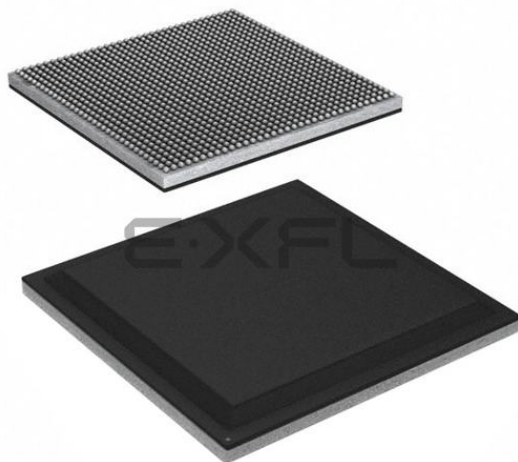




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-2ffvc1156i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
PL System Monitor					
V _{CCADC}	PL System Monitor supply relative to GNDADC.	1.746	1.800	1.854	V
V _{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T _j ⁽¹³⁾	Junction temperature operating range for extended (E) temperature devices. ⁽¹⁴⁾	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.	–40	–	125	°C

Notes:

- All voltages are relative to GND.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* ([UG583](#)).
- V_{CC_PSINTFP_DDR} must be tied to V_{CC_PSINTFP}.
- Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at ±5% and 1.1V +0.07V/–0.04V depending upon the tolerances required by specific memory standards.
- Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at ±5%.
- If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX}. The V_{CC_PSAUX} maximum of 1.89V is acceptable on an unused V_{CC_PSBATT}.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)). The SYSMON temperature measurement errors (that are described in [Table 69](#) and [Table 124](#)) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
- Devices labeled with the speed/temperature grade of -2LE normally operate under Extended (E) temperature grade specifications with a maximum junction temperature of 100°C. However, E temperature grade devices can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do at 100°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Available Speed Grades and Operating Voltages

Table 3 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Overview* (DS890).

Table 3: Available Speed Grades and Operating Voltages

Speed Grade	V_{CCINT}	$V_{CC_PSINTLP}$	$V_{CC_PSINTFP}$	$V_{CC_PSINTFP_DDR}$	Units
-3E	0.90	0.90	0.90	0.90	V
-2E	0.85	0.85	0.85	0.85	V
-2I	0.85	0.85	0.85	0.85	V
-2LE	0.85	0.85	0.85	0.85	V
-1E	0.85	0.85	0.85	0.85	V
-1I	0.85	0.85	0.85	0.85	V
-1LI	0.85	0.85	0.85	0.85	V
-2LE	0.72	0.85	0.85	0.85	V
-1LI	0.72	0.85	0.85	0.85	V

DC Characteristics Over Recommended Operating Conditions

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	μ A
I_L	Input or output leakage current per pin (sample-tested). ⁽²⁾	–	–	15	μ A
C_{IN} ⁽³⁾	Die input capacitance at the pad (HP I/O).	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O).	–	–	4.75	pF
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 3.3V$.	75	–	190	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 2.5V$.	50	–	169	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.8V$.	60	–	120	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.5V$.	30	–	120	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.2V$.	10	–	100	μ A
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$.	60	–	200	μ A
	Pad pull-down (when selected) at $V_{IN} = 1.8V$.	29	–	120	μ A
$I_{CCADCONPL}$	Analog supply current for the PL SYSMON circuits in the power-up state.	–	–	8	mA
$I_{CCADCONPS}$	Analog supply current for the PS SYSMON circuits in the power-up state.	–	–	10	mA
$I_{CCADCOFFPL}$	Analog supply current for the PL SYSMON circuits in the power-down state.	–	–	1.5	mA
$I_{CCADCOFFPS}$	Analog supply current for the PS SYSMON circuits in the power-down state.	–	–	1.8	mA

Table 8: V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO_PSIO} + 0.30$	100%	-0.30	100%
$V_{CCO_PSIO} + 0.35$	100%	-0.35	75%
$V_{CCO_PSIO} + 0.40$	100%	-0.40	45%
$V_{CCO_PSIO} + 0.45$	100%	-0.45	40%
$V_{CCO_PSIO} + 0.50$	75%	-0.50	10%
$V_{CCO_PSIO} + 0.55$	75%	-0.55	6%
$V_{CCO_PSIO} + 0.60$	60%	-0.60	2%
$V_{CCO_PSIO} + 0.65$	30%	-0.65	0%
$V_{CCO_PSIO} + 0.70$	20%	-0.70	0%
$V_{CCO_PSIO} + 0.75$	10%	-0.75	0%
$V_{CCO_PSIO} + 0.80$	10%	-0.80	0%
$V_{CCO_PSIO} + 0.85$	8%	-0.85	0%
$V_{CCO_PSIO} + 0.90$	6%	-0.90	0%
$V_{CCO_PSIO} + 0.95$	6%	-0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 11: Power Supply Ramp Time (Cont'd)

Symbol	Description	Min	Max	Units
$T_{V_{CCO_PSDDR}}$	Ramp time from GND to 95% of V_{CCO_PSDDR} .	0.2	40	ms
$T_{V_{CC_PSDDR_PLL}}$	Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$.	0.2	40	ms
$T_{V_{CCO_PSIO}}$	Ramp time from GND to 95% of V_{CCO_PSIO} .	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels⁽¹⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS33	-0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	-12
LVC MOS25	-0.300	0.700	1.700	$V_{CCO_PSIO} + 0.30$	0.70	1.70	12	-12
LVC MOS18	-0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	$V_{CCO_PSIO} + 0.30$	0.45	$V_{CCO_PSIO} - 0.45$	12	-12

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels⁽¹⁾

DDR Standard	V_{IL}		V_{IH}		$V_{OL}^{(2)}$	$V_{OH}^{(2)}$	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.8 \times V_{CCO_PSDDR} - 0.150$	$0.8 \times V_{CCO_PSDDR} + 0.150$	10	-0.1
LPDDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.3 \times V_{CCO_PSDDR} - 0.150$	$0.3 \times V_{CCO_PSDDR} + 0.150$	0.1	-10
DDR3	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.175$	$0.5 \times V_{CCO_PSDDR} + 0.175$	8	-8
LPDDR3	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8
DDR3L	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 31: PS NAND NV-DDR Synchronous Performance

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
NV-DDR ⁽¹⁾	5	200	200	200	Mb/s
	4	166.6	166.6	166.6	Mb/s
	3	133.3	133.3	133.3	Mb/s
	2	100	100	100	Mb/s
	1	66.6	66.6	66.6	Mb/s
	0	40	40	40	Mb/s

Notes:

1. The PS NAND memory controller interface for NV-DDR switching characteristics meets the requirements of the ONFI 3.1 specification.

Table 32: PS NAND SDR Asynchronous Performance

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
SDR ⁽¹⁾⁽²⁾	5	50	50	50	Mb/s
	4	40	40	40	Mb/s
	3	33.3	33.3	33.3	Mb/s
	2	28.5	28.5	28.5	Mb/s
	1	20	20	20	Mb/s
	0	10	10	10	Mb/s

Notes:

1. The PS NAND memory controller interface for SDR switching characteristics meets the requirements of the ONFI 3.1 specification.
2. The NAND controller reference clock frequency maximum is 83 MHz.

Table 33: PS-PL Interface Performance

Symbol	Description	Min	Max	Units
F _{EMIOGEMCLK}	EMIO gigabit Ethernet controller maximum frequency.	–	125	MHz
F _{EMIOSDCLK}	EMIO SD controller maximum frequency.	–	25	MHz
F _{EMIOSPICLK}	EMIO SPI controller maximum frequency.	–	25	MHz
F _{EMIOTRACECLK}	EMIO trace controller maximum frequency.	–	125	MHz
F _{FCIDMACLK}	Flow control interface DMA maximum frequency.	–	333	MHz
F _{AXICLK}	Maximum AXI interface performance.	–	333	MHz
F _{DPLIVEVIDEO}	DisplayPort controller live video interface maximum frequency.	–	300	MHz

PS I2C Controller Interface

Table 47: I2C Interface⁽¹⁾

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
T _{I2CFCKL}	SCL Low time.	1.3	–	μs
T _{I2CFCKH}	SCL High time.	0.6	–	μs
T _{I2CFCKO}	SDA clock to out delay.	–	900	ns
T _{I2CFDCK}	SDA input setup time.	100	–	ns
F _{I2CFCLK}	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
T _{I2CSCKL}	SCL Low time.	4.7	–	μs
T _{I2CSCKH}	SCL High time.	4.0	–	μs
T _{I2CSCKO}	SDA clock to out delay.	–	3450	ns
T _{I2CSDCK}	SDA input setup time.	250	–	ns
F _{I2CSCLK}	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 63: PS-GTR Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX _{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: PCI Express Protocol Characteristics (PS-GTR Transceivers)⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: DisplayPort Protocol Characteristics (PS-GTR Transceivers)⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:

1. Only the transmitter is supported.

Table 67: USB 3.0 Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: Serial-GMII Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: PS SYSMON Specifications

Parameter	Comments	Conditions	Min	Typ	Max	Units
$V_{CC_PSADC} = 1.8V \pm 3\%$, $T_j = -40^\circ C$ to $100^\circ C$, typical values at $T_j = 40^\circ C$						
ADC Accuracy ($T_j = -55^\circ C$ to $125^\circ C$) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		$T_j = -55^\circ C$ to $110^\circ C$	–	–	± 3.5	$^\circ C$
		$T_j = 110^\circ C$ to $125^\circ C$	–	–	± 5	$^\circ C$
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 2.5	%

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF_DELAY_PAD_I}}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF_DELAY_O_PAD}}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I / O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Table 75: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_F	0.856	0.856	0.900	0.856	0.900	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
HSTL_I_S	0.856	0.856	0.900	0.856	0.900	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
HSUL_12_F	0.780	0.780	0.867	0.780	0.867	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
HSUL_12_S	0.780	0.780	0.867	0.780	0.867	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
LVC MOS12_F_12	0.918	0.918	0.976	0.918	0.976	1.689	1.689	1.856	1.689	1.856	1.202	1.202	1.317	1.202	1.317	ns
LVC MOS12_F_4	0.918	0.918	0.976	0.918	0.976	1.742	1.742	1.922	1.742	1.922	1.353	1.353	1.478	1.353	1.478	ns
LVC MOS12_F_8	0.918	0.918	0.976	0.918	0.976	1.714	1.714	1.879	1.714	1.879	1.292	1.292	1.432	1.292	1.432	ns
LVC MOS12_S_12	0.918	0.918	0.976	0.918	0.976	2.073	2.073	2.247	2.073	2.247	1.581	1.581	1.717	1.581	1.717	ns
LVC MOS12_S_4	0.918	0.918	0.976	0.918	0.976	1.979	1.979	2.182	1.979	2.182	1.633	1.633	1.772	1.633	1.772	ns
LVC MOS12_S_8	0.918	0.918	0.976	0.918	0.976	2.205	2.205	2.406	2.205	2.406	1.767	1.767	1.928	1.767	1.928	ns
LVC MOS15_F_12	0.905	0.905	0.958	0.905	0.958	1.713	1.713	1.892	1.713	1.892	1.275	1.275	1.428	1.275	1.428	ns
LVC MOS15_F_16	0.905	0.905	0.958	0.905	0.958	1.722	1.722	1.881	1.722	1.881	1.260	1.260	1.407	1.260	1.407	ns
LVC MOS15_F_4	0.905	0.905	0.958	0.905	0.958	1.825	1.825	1.959	1.825	1.959	1.453	1.453	1.557	1.453	1.557	ns
LVC MOS15_F_8	0.905	0.905	0.958	0.905	0.958	1.778	1.778	1.930	1.778	1.930	1.378	1.378	1.458	1.378	1.458	ns
LVC MOS15_S_12	0.905	0.905	0.958	0.905	0.958	1.991	1.991	2.139	1.991	2.139	1.516	1.516	1.648	1.516	1.648	ns
LVC MOS15_S_16	0.905	0.905	0.958	0.905	0.958	2.172	2.172	2.389	2.172	2.389	1.707	1.707	1.888	1.707	1.888	ns
LVC MOS15_S_4	0.905	0.905	0.958	0.905	0.958	2.313	2.313	2.483	2.313	2.483	1.952	1.952	2.123	1.952	2.123	ns
LVC MOS15_S_8	0.905	0.905	0.958	0.905	0.958	2.170	2.170	2.400	2.170	2.400	1.817	1.817	1.984	1.817	1.984	ns
LVC MOS18_F_12	0.915	0.915	0.958	0.915	0.958	1.805	1.805	1.962	1.805	1.962	1.383	1.383	1.471	1.383	1.471	ns
LVC MOS18_F_16	0.915	0.915	0.958	0.915	0.958	1.785	1.785	1.917	1.785	1.917	1.338	1.338	1.446	1.338	1.446	ns
LVC MOS18_F_4	0.915	0.915	0.958	0.915	0.958	1.868	1.868	2.013	1.868	2.013	1.472	1.472	1.599	1.472	1.599	ns
LVC MOS18_F_8	0.915	0.915	0.958	0.915	0.958	1.797	1.797	1.979	1.797	1.979	1.384	1.384	1.487	1.384	1.487	ns
LVC MOS18_S_12	0.915	0.915	0.958	0.915	0.958	2.201	2.201	2.408	2.201	2.408	1.762	1.762	1.894	1.762	1.894	ns
LVC MOS18_S_16	0.915	0.915	0.958	0.915	0.958	2.173	2.173	2.362	2.173	2.362	1.702	1.702	1.834	1.702	1.834	ns
LVC MOS18_S_4	0.915	0.915	0.958	0.915	0.958	2.346	2.346	2.567	2.346	2.567	1.951	1.951	2.092	1.951	2.092	ns
LVC MOS18_S_8	0.915	0.915	0.958	0.915	0.958	2.292	2.292	2.511	2.292	2.511	1.848	1.848	2.008	1.848	2.008	ns
LVC MOS25_F_12	0.988	0.988	1.042	0.988	1.042	2.153	2.153	2.453	2.153	2.453	1.692	1.692	1.856	1.692	1.856	ns
LVC MOS25_F_16	0.988	0.988	1.042	0.988	1.042	2.105	2.105	2.406	2.105	2.406	1.623	1.623	1.786	1.623	1.786	ns
LVC MOS25_F_4	0.988	0.988	1.042	0.988	1.042	2.344	2.344	2.554	2.344	2.554	1.842	1.842	2.039	1.842	2.039	ns
LVC MOS25_F_8	0.988	0.988	1.042	0.988	1.042	2.184	2.184	2.516	2.184	2.516	1.726	1.726	1.910	1.726	1.910	ns
LVC MOS25_S_12	0.988	0.988	1.042	0.988	1.042	2.558	2.558	2.840	2.558	2.840	1.971	1.971	2.194	1.971	2.194	ns
LVC MOS25_S_16	0.988	0.988	1.042	0.988	1.042	2.449	2.449	2.740	2.449	2.740	1.852	1.852	2.063	1.852	2.063	ns
LVC MOS25_S_4	0.988	0.988	1.042	0.988	1.042	2.770	2.770	3.066	2.770	3.066	2.224	2.224	2.458	2.224	2.458	ns
LVC MOS25_S_8	0.988	0.988	1.042	0.988	1.042	2.663	2.663	2.963	2.663	2.963	2.091	2.091	2.373	2.091	2.373	ns
LVC MOS33_F_12	1.154	1.154	1.213	1.154	1.213	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVC MOS33_F_16	1.154	1.154	1.213	1.154	1.213	2.383	2.383	2.603	2.383	2.603	1.734	1.734	1.869	1.734	1.869	ns
LVC MOS33_F_4	1.154	1.154	1.213	1.154	1.213	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVC MOS33_F_8	1.154	1.154	1.213	1.154	1.213	2.603	2.603	2.822	2.603	2.822	1.937	1.937	2.130	1.937	2.130	ns
LVC MOS33_S_12	1.154	1.154	1.213	1.154	1.213	2.705	2.705	3.047	2.705	3.047	2.049	2.049	2.318	2.049	2.318	ns
LVC MOS33_S_16	1.154	1.154	1.213	1.154	1.213	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVC MOS33_S_4	1.154	1.154	1.213	1.154	1.213	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns

Table 78: Input Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0 ⁽⁶⁾	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

PLL Switching Characteristics

Table 86: PLL Specification⁽¹⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F _{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3					
PLL_T _{OUTDUTY}	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100					μs
PLL_F _{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. ⁽⁵⁾	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_F _{BANDWIDTH}	PLL bandwidth at typical.	14	14	14	14	14	MHz
PLL_F _{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 90](#) and [Table 91](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T _{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU2}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU3}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU4}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU5}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU6}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T _{PHFD_ZU7}		Hold		−0.40	−0.40	−0.40	−0.21	−0.21	ns
T _{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU9}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU11}		Hold		−0.29	−0.29	−0.29	−0.09	0.19	ns
T _{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T _{PHFD_ZU15}		Hold		−0.04	−0.04	−0.04	0.27	0.43	ns
T _{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T _{PHFD_ZU17}		Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns
T _{PSFD_ZU19}	Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns	
T _{PHFD_ZU19}	Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 93: Package Skew

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCZU2	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU3	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU4	SFVC784		ps
			FBVB900		ps
		XCZU5	SFVC784		ps
			FBVB900		ps
		XCZU6	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU7	FBVB900	141	ps
			FFVC1156	175	ps
			FFVF1517	305	ps
		XCZU9	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU11	FFVC1156		ps
			FFVB1517		ps
			FFVF1517		ps
			FFVC1760	215	ps
		XCZU15	FFVC900	118	ps
			FFVB1156	132	ps
		XCZU17	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps
		XCZU19	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

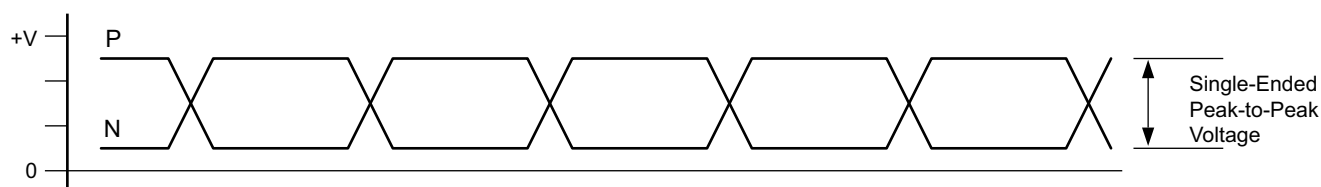
[Table 94](#) summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 94: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage.	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽³⁾		–	100	–	nF

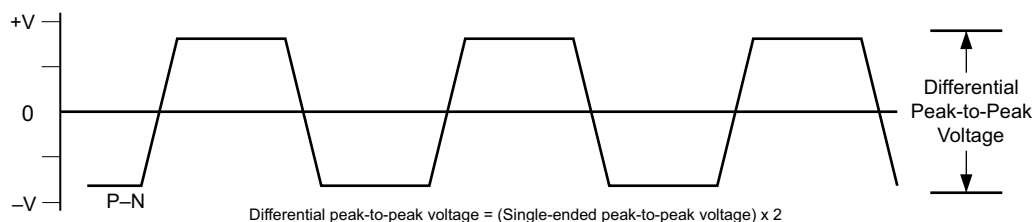
Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.



X16653-101316

Figure 5: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 6: Differential Peak-to-Peak Voltage

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 107: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale+ Interlaken](#). The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 118](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 119](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 120](#)).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See [Table 109](#) for the F_{GTYMAX} description.

Table 118: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	
F _{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F _{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 119: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V			0.72V					
		-3 ⁽¹⁾	-2 ⁽¹⁾	-1	-2	-1						
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	250.00	N/A	MHz					
		Min ⁽²⁾	Max	Min ⁽²⁾	Max	Min	Max	Min ⁽²⁾	Max	Min	Max	
F _{CORE_CLK}	Interlaken core clock	412.50 ⁽³⁾	479.20	412.50 ⁽³⁾	479.20	N/A	412.50	429.69	N/A	MHz		
F _{LBUS_CLK}	Interlaken local bus clock	300.00 ⁽⁴⁾	349.52	300.00 ⁽⁴⁾	349.52	N/A	300.00	349.52	N/A	MHz		

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F _{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F _{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Video Codec Performance

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 123: VCU Performance

Description	Speed Grade and V _{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 124: PL SYSMON Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ±3%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 5.2 MHz, T _j = −40°C to 100°C, typical values at T _j = 40°C						
ADC Accuracy ⁽¹⁾						
Resolution			10	–	–	Bits
Integral nonlinearity ⁽²⁾	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T _j = −55°C to 125°C	10	–	–	Bits
Integral nonlinearity ⁽²⁾	INL	T _j = −55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic (T _j = −55°C to 125°C)	–	–	±1	
Analog Inputs ⁽²⁾						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V