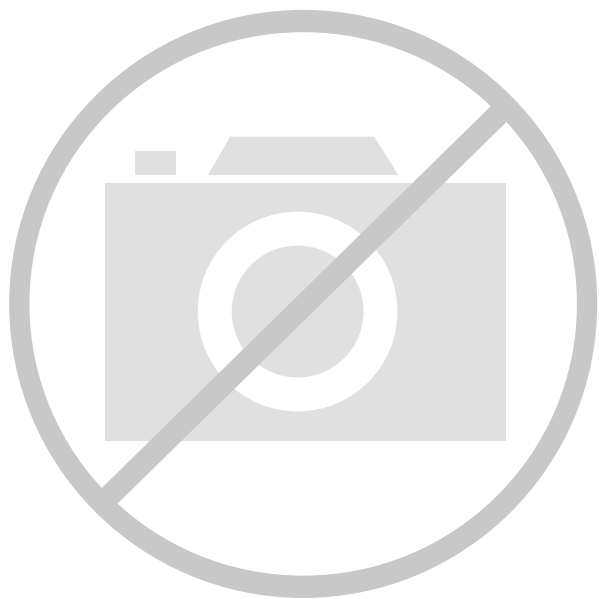




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz, 667MHz, 1.5GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-3ffvc1760e

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
V _{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
V _{CC_PSDDR_PLL}	PS DDR PLL supply voltage.	–0.500	2.000	V
V _{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V _{PSIN} ⁽²⁾	PS I/O input voltage.	–0.500	V _{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V _{CCO_PSDDR} + 0.550	V
V _{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V _{CCINT}	Internal supply voltage.	–0.500	1.000	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V _{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V _{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V _{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	–0.500	2.000	V
V _{CCAUX_IO} ⁽⁴⁾	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V _{REF}	Input reference voltage.	–0.500	2.000	V
V _{IN} ⁽²⁾⁽⁵⁾⁽⁷⁾	I/O input voltage for HD I/O banks. ⁽⁶⁾	–0.550	V _{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	–0.550	V _{CCO} + 0.550	V
I _{DC}	Available output current at the pad.	–20	20	mA
I _{RMS}	Available RMS output current at the pad.	–20	20	mA
GTH or GTY Transceiver				
V _{MGTAVCC}	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
V _{MGTAVTT}	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
V _{MGTVCCAUX}	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
V _{MGTREFCLK}	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
V _{MGTAVTTRCAL}	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V _{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating. ⁽⁸⁾	–	10	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT} .	–	10	mA
I _{DCIN-GND}	DC input current for receiver input pins DC coupled RX termination = GND. ⁽⁹⁾	–	0	mA
I _{DCIN-PROG}	DC input current for receiver input pins DC coupled RX termination = programmable. ⁽¹⁰⁾	–	0	mA
I _{DCOUT-FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
I _{DCOUT-MGTAVTT}	DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} .	–	6	mA

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Video Codec Unit				
V _{CCINT_VCU}	Internal supply voltage for the video codec unit.	−0.500	1.000	V
PL System Monitor				
V _{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V _{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T _{STG}	Storage temperature (ambient).	−65	150	°C
T _{SOL}	Maximum soldering temperature. ⁽¹²⁾	–	260	°C
T _j	Maximum junction temperature. ⁽¹²⁾	–	125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
- AC coupled operation is not supported for RX termination = floating.
- For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
- DC coupled operation is not supported for RX termination = programmable.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
- For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 9: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (Cont'd)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current.	XCZU2	N/A	26	26	26	26	mA
		XCZU3	N/A	26	26	26	26	mA
		XCZU4	32	32	32	32	32	mA
		XCZU5	32	32	32	32	32	mA
		XCZU6	33	33	33	33	33	mA
		XCZU7	56	56	56	56	56	mA
		XCZU9	33	33	33	33	33	mA
		XCZU11	56	56	56	56	56	mA
		XCZU15	33	33	33	33	33	mA
		XCZU17	74	74	74	74	74	mA
		XCZU19	74	74	74	74	74	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current.	XCZU2	N/A	6	6	6	6	mA
		XCZU3	N/A	6	6	6	6	mA
		XCZU4	9	9	9	9	9	mA
		XCZU5	9	9	9	9	9	mA
		XCZU6	25	24	24	24	24	mA
		XCZU7	16	15	15	15	15	mA
		XCZU9	25	24	24	24	24	mA
		XCZU11	23	22	22	22	22	mA
		XCZU15	29	28	28	28	28	mA
		XCZU17	37	35	35	35	35	mA
		XCZU19	37	35	35	35	35	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Table 11: Power Supply Ramp Time (Cont'd)

Symbol	Description	Min	Max	Units
$T_{V_{CCO_PSDDR}}$	Ramp time from GND to 95% of V_{CCO_PSDDR} .	0.2	40	ms
$T_{V_{CC_PSDDR_PLL}}$	Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$.	0.2	40	ms
$T_{V_{CCO_PSIO}}$	Ramp time from GND to 95% of V_{CCO_PSIO} .	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels⁽¹⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS33	-0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	-12
LVC MOS25	-0.300	0.700	1.700	$V_{CCO_PSIO} + 0.30$	0.70	1.70	12	-12
LVC MOS18	-0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	$V_{CCO_PSIO} + 0.30$	0.45	$V_{CCO_PSIO} - 0.45$	12	-12

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels⁽¹⁾

DDR Standard	V_{IL}		V_{IH}		$V_{OL}^{(2)}$	$V_{OH}^{(2)}$	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.8 \times V_{CCO_PSDDR} - 0.150$	$0.8 \times V_{CCO_PSDDR} + 0.150$	10	-0.1
LPDDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.3 \times V_{CCO_PSDDR} - 0.150$	$0.3 \times V_{CCO_PSDDR} + 0.150$	0.1	-10
DDR3	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.175$	$0.5 \times V_{CCO_PSDDR} + 0.175$	8	-8
LPDDR3	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8
DDR3L	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 25](#).

Table 25: Speed Specification Version By Device

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	—	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	—	16.5	MHz
$T_{TTCICLKHL}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$T_{TTCICLKHL}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	—	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	—	100	MHz

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the [AC Switching Characteristics, page 22](#). In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: LVDS Component Mode Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8) ⁽¹⁾	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4) ⁽¹⁾	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: LVDS Native Mode Performance⁽¹⁾⁽²⁾

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3 ⁽³⁾		-2 ⁽³⁾		-1		-2 ⁽³⁾		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE) ⁽⁴⁾	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE) ⁽⁴⁾	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the [High-Speed SelectIO Interface Wizard](#) available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

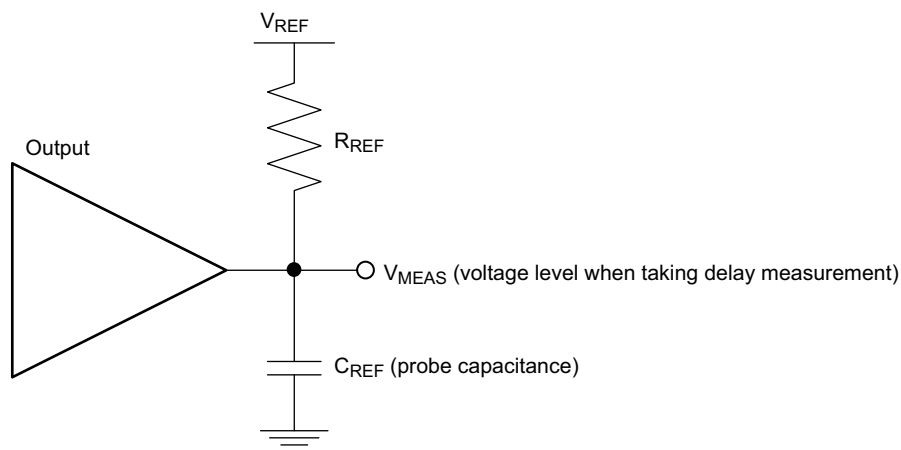
Table 77 specifies the values of $T_{\text{OUTBUF_DELAY_TE_PAD}}$ and $T_{\text{INBUF_DELAY_IBUFDIS_O}}$. $T_{\text{OUTBUF_DELAY_TE_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{\text{INBUF_DELAY_IBUFDIS_O}}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{\text{OUTBUF_DELAY_TE_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{\text{OUTBUF_DELAY_TE_PAD}}$ when the INTERMDISABLE pin is used.

Table 77: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
T _{OUTBUF_DELAY_TE_PAD}	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
T _{INBUF_DELAY_IBUFDIS_O}	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

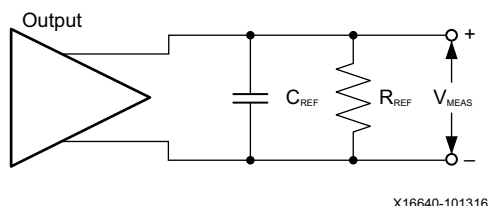
Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-101316

Figure 1: Single-Ended Test Setup



X16640-101316

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 79](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 79: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V _{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V _{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V _{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V _{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
POD10, 1.0V	POD10	50	0	V _{REF}	1.0
POD12, 1.2V	POD12	50	0	V _{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V _{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V _{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V _{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V _{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V _{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V _{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V _{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 ⁽²⁾	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 ⁽²⁾	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 ⁽²⁾	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 87 through Table 89 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.								
T _{ICKOF}	Global clock input and output flip-flop <i>without</i> MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
XCZU19	5.72	6.90	7.40	7.62	8.07	ns		

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 91: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T _{PSMMCMCC_ZU2}	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU2}		Hold			−0.19	−0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU3}		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU3}		Hold			−0.19	−0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU4}		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU4}		Hold		−0.12	−0.12	−0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU5}		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU5}		Hold		−0.12	−0.12	−0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU6}		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU6}		Hold		−0.11	−0.11	−0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU7}		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
T _{PHMMCMCC_ZU7}		Hold		−0.14	−0.14	−0.14	0.37	0.38	ns
T _{PSMMCMCC_ZU9}		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU9}		Hold		−0.11	−0.11	−0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU11}		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
T _{PHMMCMCC_ZU11}		Hold		−0.08	−0.08	0.04	0.35	0.74	ns
T _{PSMMCMCC_ZU15}		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU15}		Hold		−0.10	−0.10	−0.10	0.17	0.19	ns
T _{PSMMCMCC_ZU17}		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
T _{PHMMCMCC_ZU17}		Hold		−0.16	−0.16	−0.16	0.31	0.34	ns
T _{PSMMCMCC_ZU19}	Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns	
T _{PHMMCMCC_ZU19}	Hold		−0.16	−0.16	−0.16	0.31	0.34	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 97: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375 ⁽¹⁾		16.375 ⁽¹⁾		12.5		12.5		10.3125		Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽²⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽³⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽⁴⁾ .	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
4. The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 98: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.	250	MHz

Table 105: GTH Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽¹⁾	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽²⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽²⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI ⁽²⁾	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort ⁽²⁾	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PH-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Table 110: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTYDRPCLK}	GTYDRPCLK maximum frequency.	250	MHz

Table 111: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range.		60	–	820	MHz
T _{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask⁽¹⁾

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL _{REFCLKMASK}	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
CPLL _{REFCLKMASK}	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 116: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s	0.25	–	–	UI	
J _{T_SJ28.21}	Sinusoidal jitter (QPLL) ⁽³⁾	28.21 Gb/s	0.30	–	–	UI	
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI	
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI	
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾							
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI	
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI	
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI	
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI	

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale+ Interlaken](#). The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode ([Table 118](#)).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode ([Table 119](#)).
- 12 x 25.78125 Gb/s lane logic only mode ([Table 120](#)).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See [Table 109](#) for the F_{GTYMAX} description.

Table 118: Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	Min ⁽¹⁾	Max	
F _{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F _{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 124: PL SYSMON Specifications (Cont'd)

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error ⁽¹⁾⁽³⁾		$T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 3	$^{\circ}\text{C}$
		$T_j = -55^{\circ}\text{C}$ to 110°C (with internal REF)	–	–	± 3.5	$^{\circ}\text{C}$
		$T_j = 110^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 5	$^{\circ}\text{C}$
Supply sensor error ⁽⁴⁾		Supply voltages 0.72V to 1.2V, $T_j = -40^{\circ}\text{C}$ to 100°C (with external REF)	–	–	± 0.5	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -40^{\circ}\text{C}$ to 100°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 2.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -40^{\circ}\text{C}$ to 100°C (with internal REF)	–	–	± 1.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 2.0	%
		All other supply voltages, $T_j = -40^{\circ}\text{C}$ to 100°C (with internal REF)	–	–	± 1.5	%
		All other supply voltages, $T_j = -55^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 2.5	%
Conversion Rate⁽⁵⁾						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference⁽⁶⁾						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $T_j = -55^{\circ}\text{C}$ to 125°C	1.225	1.25	1.275	V

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- When reading temperature values directly from the PMBus interface, the SYSMON has a $+4^{\circ}\text{C}$ offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of $\pm 3^{\circ}\text{C}$ becomes $+1^{\circ}\text{C}$ to $+7^{\circ}\text{C}$ when the temperature is read through the PMBus interface.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
- See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- Any variation in the reference voltage from the nominal $V_{\text{REFP}} = 1.25\text{V}$ and $V_{\text{REFN}} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1 . Updated Table 2 , Table 4 , Table 6 , Table 7 , and Table 9 . Revised the Power Supply Sequencing section including Table 10 . Added PS and VCU ramp times to Table 11 . Revised V_{ODIFF} in Table 24 . Updated Table 25 . Added Note 1 to Table 26 . Table 30 replaces the previous three PS memory performance tables. Added values to Table 34 , Table 37 , and Table 38 . Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40 . Added Note 3 to Table 41 . Added Note 3 to Table 42 . Added Note 1 to Table 45 . Updated Table 48 and removed Note 3 . Added data to Table 56 . Updated Table 60 . Added Table 61 . Updated Table 63 . Revised Table 69 . Added data to Table 70 . Added Note 2 to Table 71 . Updated Table 74 and added Note 4 . Updated V_L and V_H values in Table 78 . Added T_{MINPER_CLK} , revised F_{REFCLK} , and Note 1 to Table 82 . Added $MMCM_F_{DPRCLK_MAX}$ to Table 85 and $PLL_F_{DPRCLK_MAX}$ to Table 86 . Added data to Table 94 , Table 96 , Table 98 , Table 101 , and updated the note references in Table 102 . Updated Table 103 and added Note 8 . Updated Table 104 and added Note 7 . Added more protocols, Note 1 and Note 2 to Table 105 . Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 105 . Added Note 1 to Table 109 . Added data to Table 106 , Table 108 , Table 110 , Table 113 . Added Note 2 to Table 112 . Added note references in Table 114 . Updated Table 115 and added Note 8 . Updated Table 116 and added Note 7 . Added more protocols and Note 3 to Table 117 . Removed the GTy Transceiver Protocol Jitter Characteristics section because it is covered in Table 117 . Revised Table 124 . Added T_{POR} and updated F_{ICAPCK} in Table 127 . Updated the Automotive Applications Disclaimer .
06/20/2016	1.1	Updated the Summary description. In Table 1 , revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU} , I_{RPD} , and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5 . Updated Note 5 in Table 4 . Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added $MIPI_DPHY_DCI$ to Table 14 , Table 15 , and Table 17 . Updated Table 23 , including removing the V_{CCO} specification and adding Note 1 . Added Note 1 to Table 24 . Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28 . Updated the -2 value in Table 29 . Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33 . Added VCO frequencies to Table 36 . Added the T_{PSPOR} minimum to Table 37 and updated Note 1 . Added Table 38 . Added value delineation over V_{CCINT} operating voltages in Table 39 . Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42 . Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43 . Added $F_{TSI_REF_CLK}$ to Table 44 and updated Note 1 . In Table 45 , revised $T_{DCSDHCLK1}$, $T_{DCSDHCLK2}$, and $T_{DCSDHCLK3}$ and Note 1 . In Table 46 , revised Note 1 . In Table 47 , revised Note 1 . Revised Table 48 , including Note 1 , and added Note 2 and Note 3 . In Table 49 , Table 50 , Table 51 , and Table 53 , revised Note 1 . Updated Table 71 . Replaced Table 74 . Updated Table 75 and Table 76 . Updated Table 78 and Table 79 . In Table 80 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95 . Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97 . Added Table 100 and Table 112 . Added Note 2 to Table 106 . Revised data in Table 109 . Revised Table 114 . Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121 . Moved Table 123 . Revised INL in Table 124 . Added notes to Table 125 and Table 126 . In the eFUSE and Programming Conditions table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.

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