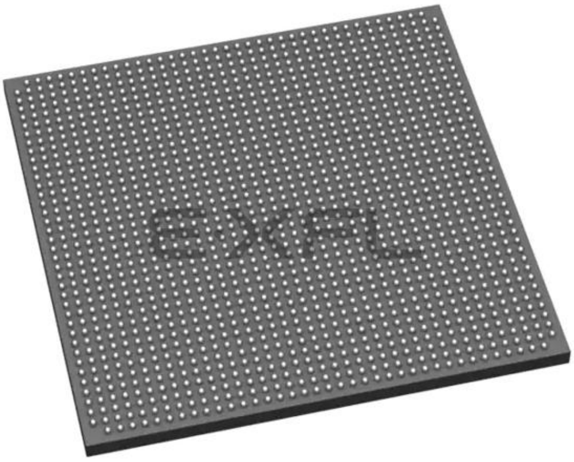
AMD Xilinx - XCZU11EG-L1FFVF1517I Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-l1ffvf1517i

Table 2: **Recommended Operating Conditions**[1][2] ***(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
PL System Monitor					
V_{CCADC}	PL System Monitor supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j[13]	Junction temperature operating range for extended (E) temperature devices.[14]	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. $V_{CC\_PSINTFP\_DDR}$ must be tied to $V_{CC\_PSINTFP}$.
4. Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at ±5% and 1.1V +0.07V/–0.04V depending upon the tolerances required by specific memory standards.
5. Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at ±5%.
6. If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX}. The V_{CC_PSAUX} maximum of 1.89V is acceptable on an unused V_{CC_PSBATT}.
7. V_{CCINT_IO} must be connected to V_{CCBRAM}.
8. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
9. V_{CCAUX_IO} must be connected to V_{CCAUX}.
10. The lower absolute voltage specification always applies.
11. A total of 200 mA per bank should not be exceeded.
12. Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
13. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 69 and Table 124) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
14. Devices labeled with the speed/temperature grade of -2LE normally operate under Extended (E) temperature grade specifications with a maximum junction temperature of 100°C. However, E temperature grade devices can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do at 100°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[(1)]	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **PS MIO Pull-up and Pull-down Current**

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 3.3V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 2.5V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 1.8V.	15	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	15	65	µA

Quiescent Supply Current

Table 9: **Typical Quiescent Supply Current**(1)(2)(3)(4)

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCZU2	N/A	393	393	344	344	mA
		XCZU3	N/A	393	393	344	344	mA
		XCZU4	719	684	684	601	601	mA
		XCZU5	719	684	684	601	601	mA
		XCZU6	1629	1549	1549	1358	1358	mA
		XCZU7	1263	1201	1201	1055	1055	mA
		XCZU9	1629	1549	1549	1358	1358	mA
		XCZU11	1786	1699	1699	1491	1491	mA
		XCZU15	1987	1890	1890	1660	1660	mA
		XCZU17	2728	2594	2594	2275	2275	mA
		XCZU19	2728	2594	2594	2275	2275	mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current.	XCZU2	N/A	44	44	44	44	mA
		XCZU3	N/A	44	44	44	44	mA
		XCZU4	61	59	59	59	59	mA
		XCZU5	61	59	59	59	59	mA
		XCZU6	61	59	59	59	59	mA
		XCZU7	120	115	115	115	115	mA
		XCZU9	61	59	59	59	59	mA
		XCZU11	120	115	115	115	115	mA
		XCZU15	61	59	59	59	59	mA
		XCZU17	164	158	158	158	158	mA
		XCZU19	164	158	158	158	158	mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	All devices	1	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCZU2	N/A	55	55	55	55	mA
		XCZU3	N/A	55	55	55	55	mA
		XCZU4	90	90	90	90	90	mA
		XCZU5	90	90	90	90	90	mA
		XCZU6	227	227	227	227	227	mA
		XCZU7	174	174	174	174	174	mA
		XCZU9	227	227	227	227	227	mA
		XCZU11	255	255	255	255	255	mA
		XCZU15	266	266	266	266	266	mA
		XCZU17	396	396	396	396	396	mA
		XCZU19	396	396	396	396	396	mA

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 10: **Power-on Current by Device**[(1)]

I_{CC} Min =	I_{CCQ} +	XCZU2	XCZU3	XCZU4	XCZU5	XCZU6	XCZU7	XCZU9	XCZU11	XCZU15	XCZU17	XCZU19	Units
$I_{CCINTMIN}$	I_{CCINTQ} +	464	464	770	770	1800	1514	1800	1961	2242	3433	3433	mA
I_{CCINT_IOMIN} + $I_{CCBRAMMIN}$	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} +	155	155	257	257	600	505	600	654	748	1145	1145	mA
I_{CCOMIN}	I_{CCOQ} +	50	50	50	50	50	50	50	55	63	96	96	mA
$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	I_{CCAUXQ} + I_{CCAUX_IOQ} +	111	111	386	386	650	362	650	709	810	1240	1240	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

Table 11: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}.	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}.	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU}.	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}.	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}.	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}.	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms
$T_{VCC\_PSINTFP}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP}$.	0.2	40	ms
$T_{VCC\_PSINTLP}$	Ramp time from GND to 95% of $V_{CC\_PSINTLP}$.	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX}.	0.2	40	ms
$T_{VCC\_PSINTFP\_DDR}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP\_DDR}$.	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC}.	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL}.	0.2	40	ms
$T_{PS\_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVCC}$.	0.2	40	ms
$T_{PS\_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVTT}$.	0.2	40	ms

Table 11: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**[1]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:

1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**[1]

DDR Standard	V_{IL}		V_{IH}		V_{OL}[2]	V_{OH}[2]	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	**Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages**		
	Advance	**Preliminary**	**Production**
XCZU5EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU6CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU6EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU7CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU9CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU9EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

Table 37: PS Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time.(1)	10	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time.	3	–	–	PS_REF_CLK Clock Cycles

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: PS Clocks Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{TOPSW\_MAINMAX}$	TOPSW_MAIN maximum frequency.	600	533	533	MHz
$F_{TOPSW\_LSBUSMAX}$	TOPSW_LSBUS maximum frequency.	100	100	100	MHz
$F_{GDMAMAX}$	FPD-DMA maximum frequency.	600	600	600	MHz
$F_{DPDMAMAX}$	DisplayPort DMA maximum frequency.	600	600	600	MHz
$F_{LPD\_SWITCH\_CTRLMAX}$	LPD_SWITCH_CTRL maximum frequency.	600	500	500	MHz
$F_{LPD\_LSBUS\_CTRLMAX}$	LPD_LSBUS_CTRL maximum frequency.	100	100	100	MHz
$F_{ADMAMAX}$	LPD-DMA maximum frequency.	600	500	500	MHz
$F_{APLL\_TO\_LPDMAX}$	APLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{DPLL\_TO\_LPDMAX}$	DPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{VPLL\_TO\_LPDMAX}$	VPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{IOPLL\_TO\_LPDMAX}$	IOPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{RPLL\_TO\_FPDMAX}$	RPLL_TO_FPD maximum frequency.	533	533	533	MHz

PS SPI Controller Interface

Table 48: **SPI Interfaces**(1)

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: **CAN Interface**(1)

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 60: **PS-GTR Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequencies supported.	PCI Express	100 MHz			
		SATA	125 MHz or 150 MHz			
		USB 3.0	26 MHz, 52 MHz, or 100 MHz			
		DisplayPort	27 MHz, 108 MHz, or 135 MHz			
		SGMII	125 MHz			
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only.	40	–	60	%
		USB 3.0 with reference clock <40 MHz.	47.5	–	52.5	%

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					**Units**
	0.90V	**0.85V**		**0.72V**		**0.90V**	**0.85V**		**0.72V**		**0.90V**	**0.85V**		**0.72V**		
	-3	**-2**	**-1**	**-2**	**-1**	**-3**	**-2**	**-1**	**-2**	**-1**	**-3**	**-2**	**-1**	**-2**	**-1**	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 77: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 87 through Table 89 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
		XCZU19	5.72	6.90	7.40	7.62	8.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]									
$T_{PSMMCMCC\_ZU2}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU2}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU3}$		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU3}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU4}$		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU4}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU5}$		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU5}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU6}$		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU6}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU7}$		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
$T_{PHMMCMCC\_ZU7}$		Hold		–0.14	–0.14	–0.14	0.37	0.38	ns
$T_{PSMMCMCC\_ZU9}$		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU9}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU11}$		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
$T_{PHMMCMCC\_ZU11}$		Hold		–0.08	–0.08	0.04	0.35	0.74	ns
$T_{PSMMCMCC\_ZU15}$		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU15}$		Hold		–0.10	–0.10	–0.10	0.17	0.19	ns
$T_{PSMMCMCC\_ZU17}$		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU17}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns
$T_{PSMMCMCC\_ZU19}$		Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU19}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 102: **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 110: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 111: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 116: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1. Updated Table 2, Table 4, Table 6, Table 7, and Table 9. Revised the Power Supply Sequencing section including Table 10. Added PS and VCU ramp times to Table 11. Revised V_{ODIFF} in Table 24. Updated Table 25. Added Note 1 to Table 26. Table 30 replaces the previous three PS memory performance tables. Added values to Table 34, Table 37, and Table 38. Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the *PS NAND Memory Controller Interface* section. Added and updated data in Table 40. Added Note 3 to Table 41. Added Note 3 to Table 42. Added Note 1 to Table 45. Updated Table 48 and removed Note 3. Added data to Table 56. Updated Table 60. Added Table 61. Updated Table 63. Revised Table 69. Added data to Table 70. Added Note 2 to Table 71. Updated Table 74 and added Note 4. Updated V_L and V_H values in Table 78. Added T_{MINPER_CLK}, revised F_{REFCLK}, and Note 1 to Table 82. Added MMCM_F_{DPRCLK_MAX} to Table 85 and PLL_F_{DPRCLK_MAX} to Table 86. Added data to Table 94, Table 96, Table 98, Table 101, and updated the note references in Table 102. Updated Table 103 and added Note 8. Updated Table 104 and added Note 7. Added more protocols, Note 1 and Note 2 to Table 105. Removed the *GTH Transceiver Protocol Jitter Characteristics* section because it is covered in Table 105. Added Note 1 to Table 109. Added data to Table 106, Table 108, Table 110, Table 113. Added Note 2 to Table 112. Added note references in Table 114. Updated Table 115 and added Note 8. Updated Table 116 and added Note 7. Added more protocols and Note 3 to Table 117. Removed the *GTY Transceiver Protocol Jitter Characteristics* section because it is covered in Table 117. Revised Table 124. Added T_{POR} and updated F_{ICAPCK} in Table 127. Updated the Automotive Applications Disclaimer.
06/20/2016	1.1	Updated the Summary description. In Table 1, revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU}, I_{RPD}, and Note 4 to Table 2 and updated $V_{PS\_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 4. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 14, Table 15, and Table 17. Updated Table 23, including removing the V_{CCO} specification and adding Note 1. Added Note 1 to Table 24. Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28. Updated the -2 value in Table 29. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33. Added VCO frequencies to Table 36. Added the T_{PSPOR} minimum to Table 37 and updated Note 1. Added Table 38. Added value delineation over V_{CCINT} operating voltages in Table 39. Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the *PS NAND Memory Controller Interface* section. Revised some units and Note 1 in Table 41 and Table 42. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43. Added $F_{TSI\_REF\_CLK}$ to Table 44 and updated Note 1. In Table 45, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 46, revised Note 1. In Table 47, revised Note 1. Revised Table 48, including Note 1, and added Note 2 and Note 3. In Table 49, Table 50, Table 51, and Table 53, revised Note 1. Updated Table 71. Replaced Table 74. Updated Table 75 and Table 76. Updated Table 78 and Table 79. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97. Added Table 100 and Table 112. Added Note 2 to Table 106. Revised data in Table 109. Revised Table 114. Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121. Moved Table 123. Revised INL in Table 124. Added notes to Table 125 and Table 126. In the *eFUSE and Programming Conditions* table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.