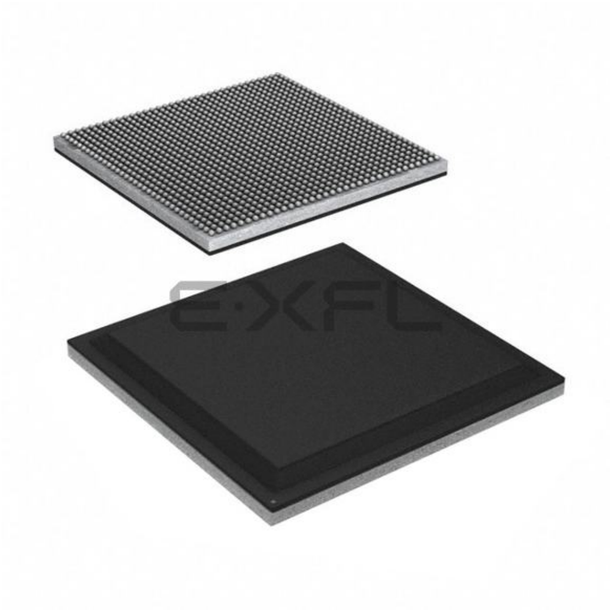
AMD Xilinx - XCZU11EG-L2FFVC1156E Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 653K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu11eg-l2ffvc1156e

Available Speed Grades and Operating Voltages

Table 3 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Overview* (DS890).

Table 3: **Available Speed Grades and Operating Voltages**

Speed Grade	V_{CCINT}	$V_{CC\_PSINTLP}$	$V_{CC\_PSINTFP}$	$V_{CC\_PSINTFP\_DDR}$	Units
-3E	0.90	0.90	0.90	0.90	V
-2E	0.85	0.85	0.85	0.85	V
-2I	0.85	0.85	0.85	0.85	V
-2LE	0.85	0.85	0.85	0.85	V
-1E	0.85	0.85	0.85	0.85	V
-1I	0.85	0.85	0.85	0.85	V
-1LI	0.85	0.85	0.85	0.85	V
-2LE	0.72	0.85	0.85	0.85	V
-1LI	0.72	0.85	0.85	0.85	V

DC Characteristics Over Recommended Operating Conditions

Table 4: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested).(2)	–	–	15	µA
C_{IN}(3)	Die input capacitance at the pad (HP I/O).	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O).	–	–	4.75	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	29	–	120	µA
$I_{CCADCONPL}$	Analog supply current for the PL SYSMON circuits in the power-up state.	–	–	8	mA
$I_{CCADCONPS}$	Analog supply current for the PS SYSMON circuits in the power-up state.	–	–	10	mA
$I_{CCADCOFFPL}$	Analog supply current for the PL SYSMON circuits in the power-down state.	–	–	1.5	mA
$I_{CCADCOFFPS}$	Analog supply current for the PS SYSMON circuits in the power-down state.	–	–	1.8	mA

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks**[1]

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks**[1][2]

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Quiescent Supply Current

Table 9: **Typical Quiescent Supply Current**(1)(2)(3)(4)

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCZU2	N/A	393	393	344	344	mA
		XCZU3	N/A	393	393	344	344	mA
		XCZU4	719	684	684	601	601	mA
		XCZU5	719	684	684	601	601	mA
		XCZU6	1629	1549	1549	1358	1358	mA
		XCZU7	1263	1201	1201	1055	1055	mA
		XCZU9	1629	1549	1549	1358	1358	mA
		XCZU11	1786	1699	1699	1491	1491	mA
		XCZU15	1987	1890	1890	1660	1660	mA
		XCZU17	2728	2594	2594	2275	2275	mA
		XCZU19	2728	2594	2594	2275	2275	mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current.	XCZU2	N/A	44	44	44	44	mA
		XCZU3	N/A	44	44	44	44	mA
		XCZU4	61	59	59	59	59	mA
		XCZU5	61	59	59	59	59	mA
		XCZU6	61	59	59	59	59	mA
		XCZU7	120	115	115	115	115	mA
		XCZU9	61	59	59	59	59	mA
		XCZU11	120	115	115	115	115	mA
		XCZU15	61	59	59	59	59	mA
		XCZU17	164	158	158	158	158	mA
		XCZU19	164	158	158	158	158	mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	All devices	1	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCZU2	N/A	55	55	55	55	mA
		XCZU3	N/A	55	55	55	55	mA
		XCZU4	90	90	90	90	90	mA
		XCZU5	90	90	90	90	90	mA
		XCZU6	227	227	227	227	227	mA
		XCZU7	174	174	174	174	174	mA
		XCZU9	227	227	227	227	227	mA
		XCZU11	255	255	255	255	255	mA
		XCZU15	266	266	266	266	266	mA
		XCZU17	396	396	396	396	396	mA
		XCZU19	396	396	396	396	396	mA

Table 11: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**[(1)]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:

1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**[(1)]

DDR Standard	V_{IL}		V_{IH}		V_{OL}[(2)]	V_{OH}[(2)]	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

PL I/O Levels

Table 14: **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU5EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU6CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU6EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU7CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU9CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU9EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)

Table 45: **SD/SDIO Interface(1)** ***(Cont'd)***

Symbol	Description	Min	Max	Units
$F_{SDSDRCLK2}$	SDR50 mode device clock frequency.	–	100	MHz
	SDR25 mode device clock frequency.	–	50	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs.	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs.	24.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle.	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs.(2)	2.2	13.8	ns
$T_{SDHSDIVW}$	Input valid data window.(3)	0.35	–	UI
$F_{SDHSCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle.	45	55	%
T_{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs.	2.0	–	ns
$F_{SDIDCLK}$	Clock frequency in identification mode.	–	400	KHz
F_{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS DAP Interface

Table 50: **DAP Interface**[1]

Symbol	Description[2]	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time.	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time.	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay.	–	10.86	ns
$T_{PDAPCLK}$	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: **UART Interface**[1]

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate.	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate.	–	6.25	Mb/s
$F_{UART\_REF\_CLK}$	UART reference clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: **General Purpose I/O (GPIO) Interface**

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width.	$10 \times 1/F_{LPD\_LSBUS\_CTRLMAX}$	–	µs
$T_{PWGPIOL}$	Input Low pulse width.	$10 \times 1/F_{LPD\_LSBUS\_CTRLMAX}$	–	µs

PS Trace Interface

Table 53: **Trace Interface**[1]

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle.	45	55	%
F_{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS-GTR Transceiver

Table 56: **PS-GTR Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.		75	–	$V_{PS\_MGTRAVCC}$	mV
V_{CMIN}	Common mode input voltage.		–	0	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.(1)	Transmitter output swing is set to maximum value.	800	–	–	mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{PS\_MGTRAVCC} – D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
$R_{MGTRREF}$	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–	20	ps
C_{EXT}	Recommended external AC coupling capacitor.(2)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: **PS-GTR Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 58: **PS-GTR Transceiver Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTRMAX}	PS-GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F_{GTRMIN}	PS-GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 59: **PS-GTR Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock.	–	–	0.11	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24×10^6	UI

Table 63: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX_{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: **PCI Express Protocol Characteristics (PS-GTR Transceivers)**(1)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: **DisplayPort Protocol Characteristics (PS-GTR Transceivers)**(1)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:

1. Only the transmitter is supported.

IOB High Performance (HP) Switching Characteristics

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 87 through Table 89 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
		XCZU19	5.72	6.90	7.40	7.62	8.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
$T_{PSMMCMCC\_ZU2}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU2}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU3}$		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU3}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU4}$		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU4}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU5}$		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU5}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU6}$		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU6}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU7}$		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
$T_{PHMMCMCC\_ZU7}$		Hold		–0.14	–0.14	–0.14	0.37	0.38	ns
$T_{PSMMCMCC\_ZU9}$		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU9}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU11}$		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
$T_{PHMMCMCC\_ZU11}$		Hold		–0.08	–0.08	0.04	0.35	0.74	ns
$T_{PSMMCMCC\_ZU15}$		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU15}$		Hold		–0.10	–0.10	–0.10	0.17	0.19	ns
$T_{PSMMCMCC\_ZU17}$		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU17}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns
$T_{PSMMCMCC\_ZU19}$		Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU19}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 92: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T_{SAMP_BUFG}[1]	510	610	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	150	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	110	ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Table 104: **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 105. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

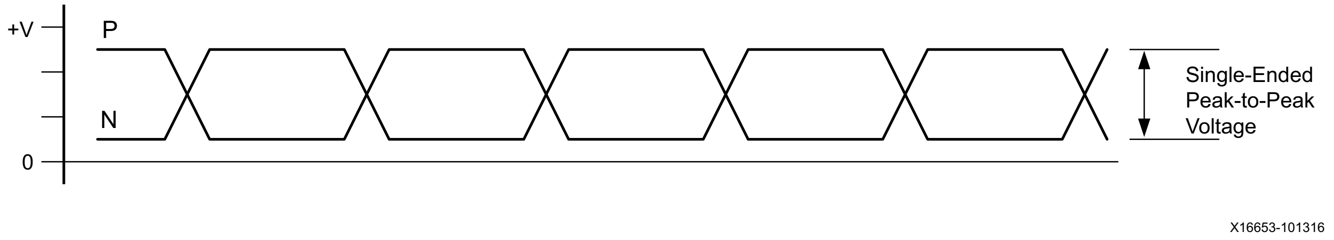

Figure 5: **Single-Ended Peak-to-Peak Voltage**

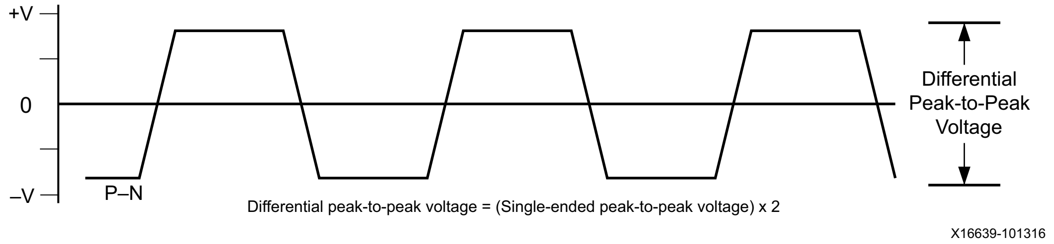

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

Table 110: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 111: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades Min	Typ	Max	Units
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 117. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(2)	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(3)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(3)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3[1]		-2[1]		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min[2]	Max	Min[2]	Max	Min	Max	Min[2]	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50[3]	479.20	412.50[3]	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00[4]	349.52	300.00[4]	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz