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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 747K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu15eg-2ffvc900i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
V _{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
V _{CC_PSDDR_PLL}	PS DDR PLL supply voltage.	–0.500	2.000	V
V _{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V _{PSIN} ⁽²⁾	PS I/O input voltage.	–0.500	V _{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V _{CCO_PSDDR} + 0.550	V
V _{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V _{CCINT}	Internal supply voltage.	–0.500	1.000	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V _{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V _{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V _{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	–0.500	2.000	V
V _{CCAUX_IO} ⁽⁴⁾	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V _{REF}	Input reference voltage.	–0.500	2.000	V
V _{IN} ⁽²⁾⁽⁵⁾⁽⁷⁾	I/O input voltage for HD I/O banks. ⁽⁶⁾	–0.550	V _{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	–0.550	V _{CCO} + 0.550	V
I _{DC}	Available output current at the pad.	–20	20	mA
I _{RMS}	Available RMS output current at the pad.	–20	20	mA
GTH or GTY Transceiver				
V _{MGTAVCC}	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
V _{MGTAVTT}	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
V _{MGTVCCAUX}	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
V _{MGTREFCLK}	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
V _{MGTAVTTRCAL}	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V _{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating. ⁽⁸⁾	–	10	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT} .	–	10	mA
I _{DCIN-GND}	DC input current for receiver input pins DC coupled RX termination = GND. ⁽⁹⁾	–	0	mA
I _{DCIN-PROG}	DC input current for receiver input pins DC coupled RX termination = programmable. ⁽¹⁰⁾	–	0	mA
I _{DCOUT-FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
I _{DCOUT-MGTAVTT}	DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} .	–	6	mA

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Video Codec Unit				
V _{CCINT_VCU}	Internal supply voltage for the video codec unit.	−0.500	1.000	V
PL System Monitor				
V _{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V _{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T _{STG}	Storage temperature (ambient).	−65	150	°C
T _{SOL}	Maximum soldering temperature. ⁽¹²⁾	–	260	°C
T _j	Maximum junction temperature. ⁽¹²⁾	–	125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
- AC coupled operation is not supported for RX termination = floating.
- For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
- DC coupled operation is not supported for RX termination = programmable.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
- For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTAVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 15: SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	5.8	−5.8
HSTL_I_12	−0.300	V _{REF} − 0.080	V _{REF} + 0.080	V _{CCO} + 0.300	25% V _{CCO}	75% V _{CCO}	4.1	−4.1
HSTL_I_18	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	6.2	−6.2
HSUL_12	−0.300	V _{REF} − 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.1	−0.1
LVC MOS12	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	Note 4	Note 4
LVC MOS15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVC MOS18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVDCI_15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
LVDCI_18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
SSTL12	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	8.0	−8.0
SSTL135	−0.300	V _{REF} − 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	9.0	−9.0
SSTL15	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.175	V _{CCO} /2 + 0.175	10.0	−10.0
SSTL18_I	−0.300	V _{REF} − 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 − 0.470	V _{CCO} /2 + 0.470	7.0	−7.0
MIPI_DPHY_DCI_LP ⁽⁶⁾	−0.300	0.550	0.880	V _{CCO} + 0.300	0.050	1.100	0.01	−0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 16](#), [Table 20](#), [Table 21](#), and [Table 22](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: DC Input Levels for Single-ended POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V _{IL}		V _{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300
POD12	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 26: Speed Grade Designations by Device (Cont'd)

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU5EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU5EV	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU6CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU6EG	-3E ($V_{CCINT} = 0.90V$) -2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU7CG	-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU7EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU7EV	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU9CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU9EG	-3E ($V_{CCINT} = 0.90V$) -2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)

Table 37: PS Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T _{PSPOR}	Required PS_POR_B assertion time. ⁽¹⁾	10	–	–	μs
T _{PSRST}	Required PS_SRST_B assertion time.	3	–	–	PS_REF_CLK Clock Cycles

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: PS Clocks Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{TOPSW_MAINMAX}	TOPSW_MAIN maximum frequency.	600	533	533	MHz
F _{TOPSW_LSBUSMAX}	TOPSW_LSBUS maximum frequency.	100	100	100	MHz
F _{GDMAMAX}	FPD-DMA maximum frequency.	600	600	600	MHz
F _{DPMAMAX}	DisplayPort DMA maximum frequency.	600	600	600	MHz
F _{LPD_SWITCH_CTRLMAX}	LPD_SWITCH_CTRL maximum frequency.	600	500	500	MHz
F _{LPD_LSBUS_CTRLMAX}	LPD_LSBUS_CTRL maximum frequency.	100	100	100	MHz
F _{ADMAMAX}	LPD-DMA maximum frequency.	600	500	500	MHz
F _{APLL_TO_LPDMAX}	APLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{DPLL_TO_LPDMAX}	DPLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{VPDLL_TO_LPDMAX}	VPLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{IOPLL_TO_LPDMAX}	IOPLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{RPLL_TO_FPDMAX}	RPLL_TO_FPD maximum frequency.	533	533	533	MHz

PS Configuration

Table 39: Processor Configuration Access Port Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: Boundary-Scan Port Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS DAP Interface

Table 50: DAP Interface⁽¹⁾

Symbol	Description ⁽²⁾	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time.	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time.	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay.	–	10.86	ns
$T_{PDAPCLK}$	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: UART Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate.	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate.	–	6.25	Mb/s
$F_{UART_REF_CLK}$	UART reference clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: General Purpose I/O (GPIO) Interface

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s
$T_{PWGPIOL}$	Input Low pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s

PS Trace Interface

Table 53: Trace Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle.	45	55	%
F_{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3(1)	-2(1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Table 75: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS33_S_8	1.154	1.154	1.213	1.154	1.213	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
LVDS_25	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.164	1.223	1.164	1.223	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVTTL_F_16	1.164	1.164	1.223	1.164	1.223	2.464	2.464	2.732	2.464	2.732	1.750	1.750	1.986	1.750	1.986	ns
LVTTL_F_4	1.164	1.164	1.223	1.164	1.223	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVTTL_F_8	1.164	1.164	1.223	1.164	1.223	2.582	2.582	2.787	2.582	2.787	1.910	1.910	2.063	1.910	2.063	ns
LVTTL_S_12	1.164	1.164	1.223	1.164	1.223	2.731	2.731	3.075	2.731	3.075	2.072	2.072	2.343	2.072	2.343	ns
LVTTL_S_16	1.164	1.164	1.223	1.164	1.223	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVTTL_S_4	1.164	1.164	1.223	1.164	1.223	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns
LVTTL_S_8	1.164	1.164	1.223	1.164	1.223	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
SLVS_400_25	1.020	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.780	0.867	0.780	0.867	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
SSTL12_S	0.780	0.780	0.867	0.780	0.867	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
SSTL135_F	0.798	0.798	0.881	0.798	0.881	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
SSTL135_II_F	0.798	0.798	0.881	0.798	0.881	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
SSTL135_II_S	0.798	0.798	0.881	0.798	0.881	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
SSTL135_S	0.798	0.798	0.881	0.798	0.881	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
SSTL15_F	0.838	0.838	0.880	0.838	0.880	1.612	1.612	1.754	1.612	1.754	1.357	1.357	1.464	1.357	1.464	ns
SSTL15_II_F	0.838	0.838	0.880	0.838	0.880	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
SSTL15_II_S	0.838	0.838	0.880	0.838	0.880	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
SSTL15_S	0.838	0.838	0.880	0.838	0.880	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
SSTL18_II_F	0.947	0.947	1.021	0.947	1.021	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
SSTL18_II_S	0.947	0.947	1.021	0.947	1.021	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
SSTL18_I_F	0.947	0.947	1.021	0.947	1.021	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
SSTL18_I_S	0.947	0.947	1.021	0.947	1.021	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
SUB_LVDS	1.002	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

IOB High Performance (HP) Switching Characteristics

Table 76: IOB High Performance (HP) Switching Characteristics

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

DSP48 Slice Switching Characteristics

Table 83: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	With all registers used.	891	775	645	644	600	MHz
F _{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	635	544	456	440	413	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG.	655	565	468	453	423	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 84: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F _{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F _{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F _{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Table 85: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

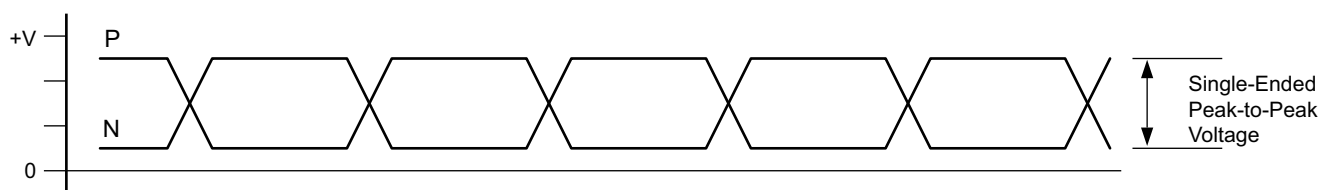
The pin-to-pin numbers in [Table 87](#) through [Table 89](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.								
T _{ICKOF}	Global clock input and output flip-flop <i>without</i> MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
XCZU19	5.72	6.90	7.40	7.62	8.07	ns		

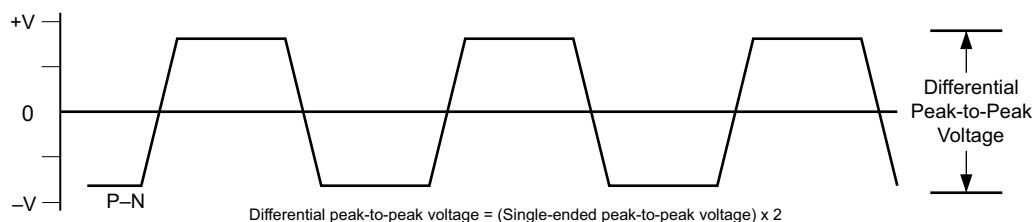
Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.



X16653-101316

Figure 3: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 4: Differential Peak-to-Peak Voltage

Table 95 and Table 96 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 95: GTH Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 96: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N.	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N.	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage. (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage.	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

[Table 106](#) and [Table 107](#) summarize the DC specifications of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 106: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 117: GTY Transceiver Protocol List (Cont'd)

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant ⁽³⁾
Fibre channel	FC-PH-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1 . Updated Table 2 , Table 4 , Table 6 , Table 7 , and Table 9 . Revised the Power Supply Sequencing section including Table 10 . Added PS and VCU ramp times to Table 11 . Revised V_{ODIFF} in Table 24 . Updated Table 25 . Added Note 1 to Table 26 . Table 30 replaces the previous three PS memory performance tables. Added values to Table 34 , Table 37 , and Table 38 . Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40 . Added Note 3 to Table 41 . Added Note 3 to Table 42 . Added Note 1 to Table 45 . Updated Table 48 and removed Note 3 . Added data to Table 56 . Updated Table 60 . Added Table 61 . Updated Table 63 . Revised Table 69 . Added data to Table 70 . Added Note 2 to Table 71 . Updated Table 74 and added Note 4 . Updated V_L and V_H values in Table 78 . Added T_{MINPER_CLK} , revised F_{REFCLK} , and Note 1 to Table 82 . Added $MMCM_F_{DPRCLK_MAX}$ to Table 85 and $PLL_F_{DPRCLK_MAX}$ to Table 86 . Added data to Table 94 , Table 96 , Table 98 , Table 101 , and updated the note references in Table 102 . Updated Table 103 and added Note 8 . Updated Table 104 and added Note 7 . Added more protocols, Note 1 and Note 2 to Table 105 . Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 105 . Added Note 1 to Table 109 . Added data to Table 106 , Table 108 , Table 110 , Table 113 . Added Note 2 to Table 112 . Added note references in Table 114 . Updated Table 115 and added Note 8 . Updated Table 116 and added Note 7 . Added more protocols and Note 3 to Table 117 . Removed the GTy Transceiver Protocol Jitter Characteristics section because it is covered in Table 117 . Revised Table 124 . Added T_{POR} and updated F_{ICAPCK} in Table 127 . Updated the Automotive Applications Disclaimer .
06/20/2016	1.1	Updated the Summary description. In Table 1 , revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU} , I_{RPD} , and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5 . Updated Note 5 in Table 4 . Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added $MIPI_DPHY_DCI$ to Table 14 , Table 15 , and Table 17 . Updated Table 23 , including removing the V_{CCO} specification and adding Note 1 . Added Note 1 to Table 24 . Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28 . Updated the -2 value in Table 29 . Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33 . Added VCO frequencies to Table 36 . Added the T_{PSPOR} minimum to Table 37 and updated Note 1 . Added Table 38 . Added value delineation over V_{CCINT} operating voltages in Table 39 . Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42 . Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43 . Added $F_{TSI_REF_CLK}$ to Table 44 and updated Note 1 . In Table 45 , revised $T_{DCSDHCLK1}$, $T_{DCSDHCLK2}$, and $T_{DCSDHCLK3}$ and Note 1 . In Table 46 , revised Note 1 . In Table 47 , revised Note 1 . Revised Table 48 , including Note 1 , and added Note 2 and Note 3 . In Table 49 , Table 50 , Table 51 , and Table 53 , revised Note 1 . Updated Table 71 . Replaced Table 74 . Updated Table 75 and Table 76 . Updated Table 78 and Table 79 . In Table 80 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95 . Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97 . Added Table 100 and Table 112 . Added Note 2 to Table 106 . Revised data in Table 109 . Revised Table 114 . Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121 . Moved Table 123 . Revised INL in Table 124 . Added notes to Table 125 and Table 126 . In the eFUSE and Programming Conditions table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.