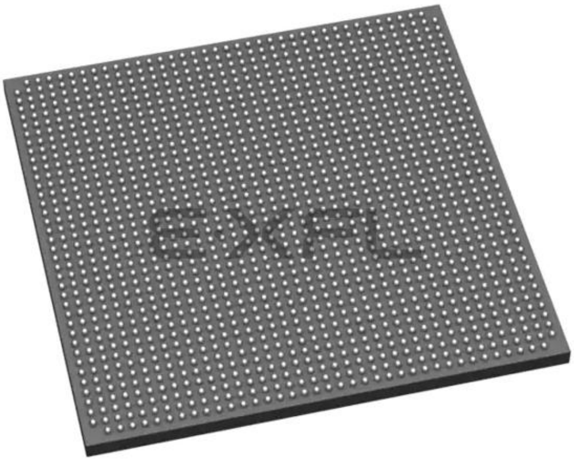

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-1ffvb1517e

Table 1: **Absolute Maximum Ratings[1]** ***(Cont'd)***

Symbol	Description	Min	Max	Units
V_{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	–0.500	2.000	V
V_{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V_{PSIN}[2]	PS I/O input voltage.	–0.500	V_{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V_{CCO_PSDDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage.	–0.500	1.000	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	–0.500	2.000	V
V_{CCAUX_IO}[4]	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V_{REF}	Input reference voltage.	–0.500	2.000	V
V_{IN}[2][5][7]	I/O input voltage for HD I/O banks.[6]	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	–0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad.	–20	20	mA
I_{RMS}	Available RMS output current at the pad.	–20	20	mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.[8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.[9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–	6	mA

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions**[1][2]

Symbol	Description	Min	Typ	Max	Units
Processor System					
$V_{CC\_PSINTFP}$[3]	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
$V_{CC\_PSINTFP\_DDR}$[3]	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage.	0.825	0.850	0.875	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage.	1.746	1.800	1.854	V
V_{CCO_PSDDR}[4]	PS DDR I/O supply voltage.	1.06	–	1.575	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V_{CCO_PSIO}[5]	PS I/O supply.	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage.	–0.200	–	V_{CCO_PSIO} + 0.200	V
	PS DDR I/O input voltage.	–0.200	–	V_{CCO_PSDDR} + 0.200	
V_{CC_PSBATT}[6]	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	1.200	–	1.500	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}[7]	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**[(1)]

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**[(1)]

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

PS Gigabit Ethernet Controller Interface

Table 44: **RGMII Interface** (1)

Symbol	Description	Min	Max	Units
$T_{DCGEMTXCLK}$	Transmit clock duty cycle.	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time.	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time.	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time.	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period.	400	–	ns
$T_{MDIOCKL}$	MDC low time.	160	–	ns
$T_{MDIOCKH}$	MDC high time.	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time.	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time.	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time.	–1.0	15	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency.	–	125	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency.	–	125	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: **SD/SDIO Interface** (1)

Symbol	Description	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
$T_{DCDDRCLK}$	SD device clock duty cycle.	45	55	%
$T_{SDDDRCKO1}$	Clock to output delay, data. (2)	1.0	6.8	ns
$T_{SDDRIVW}$	Input valid data window. (3)	3.5	–	ns
$T_{SDDDRDCK2}$	Input setup time, command.	4.7	–	ns
$T_{SDDDRCKD2}$	Input hold time, command.	1.5	–	ns
$T_{SDDDRCKO2}$	Clock to output delay, command.	1.0	13.8	ns
$F_{SDDDRCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface SDR104				
$T_{DCSDHSCLK1}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO1}$	Clock to output delay, all outputs. (2)	1.0	3.2	ns
$T_{SDSDR1IVW}$	Input valid data window. (3)	0.5	–	UI
$F_{SDSDRCLK1}$	SDR104 mode device clock frequency.	–	200	MHz
SD/SDIO Interface SDR50/25				
$T_{DCSDHSCLK2}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO2}$	Clock to output delay, all outputs. (2)	1.0	6.8	ns
$T_{SDSDR2IVW}$	Input valid data window. (3)	0.3	–	UI

Table 67: **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –55°C to 110°C	–	–	±3.5	°C
		T_j = 110°C to 125°C	–	–	±5	°C
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	T_j = –40°C to 125°C	–	–	±2.5	%

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces *(Cont'd)***

Memory Standard	Package[1]	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
QDR II+	All	Single rank component(7)	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L(1)(2)	V_H(1)(2)	V_{MEAS}(1)(4)(6)	V_{REF}(1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0(6)	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0(6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0(6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0(6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0(6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0(6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0(6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–

Table 88: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region).	XCZU2	N/A	5.27	5.68	5.80	6.13	ns
		XCZU3	N/A	5.27	5.68	5.80	6.13	ns
		XCZU4	5.07	6.06	6.61	6.23	7.10	ns
		XCZU5	5.07	6.06	6.61	6.23	7.10	ns
		XCZU6	5.38	6.49	6.97	7.14	7.59	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.38	6.49	6.97	7.14	7.59	ns
		XCZU11	6.18	7.41	8.11	7.66	8.99	ns
		XCZU15	5.38	6.49	6.96	7.19	7.71	ns
		XCZU17	6.21	7.53	8.07	8.36	8.90	ns
		XCZU19	6.21	7.53	8.07	8.36	8.90	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCZU2	N/A	2.22	2.43	2.96	2.94	ns
		XCZU3	N/A	2.22	2.43	2.96	2.94	ns
		XCZU4	2.47	2.47	2.78	3.04	3.35	ns
		XCZU5	2.47	2.47	2.78	3.04	3.35	ns
		XCZU6	2.15	2.15	2.36	2.86	2.86	ns
		XCZU7	2.32	2.32	2.57	3.06	3.13	ns
		XCZU9	2.15	2.15	2.36	2.86	2.86	ns
		XCZU11	2.64	2.64	2.96	3.25	3.55	ns
		XCZU15	2.18	2.18	2.38	2.88	2.90	ns
		XCZU17	2.44	2.44	2.66	3.19	3.17	ns
		XCZU19	2.44	2.44	2.66	3.19	3.17	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description	Device		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T_{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU2}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU3}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU4}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU5}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU6}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T_{PHFD_ZU7}		Hold		–0.40	–0.40	–0.40	–0.21	–0.21	ns
T_{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU9}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU11}		Hold		–0.29	–0.29	–0.29	–0.09	0.19	ns
T_{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T_{PHFD_ZU15}		Hold		–0.04	–0.04	–0.04	0.27	0.43	ns
T_{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU17}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns
T_{PSFD_ZU19}		Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU19}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

Table 94 summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 94: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT} = 1.2V$	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage.	DC coupled $V_{MGTAVTT} = 1.2V$	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.[1]	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor.[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 97: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTHMAX}	GTH maximum line rate.		16.375[1]		16.375[1]		12.5		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range[2].	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range[3].	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range[4].	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 98: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency.	250	MHz

Table 102: **GTH Transceiver User Clock Switching Characteristics(1)** ***(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)(5)	-2(3)	-1(5)	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2(6) maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2(6) maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 104: **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 105. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 113: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10^6	UI

Table 114: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)(5)	-2(3)	-1(5)	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 118).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 119).
- 12 x 25.78125 Gb/s lane logic only mode (Table 120).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 109 for the F_{GTYMAX} description.

Table 118: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min[1]	Max	Min[1]	Max	Min[1]	Max	Min[1]	Max	Min[1]	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Configuration Switching Characteristics

Table 127: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T_{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T_{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
$T_{PS\_PROG\_B}$	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max