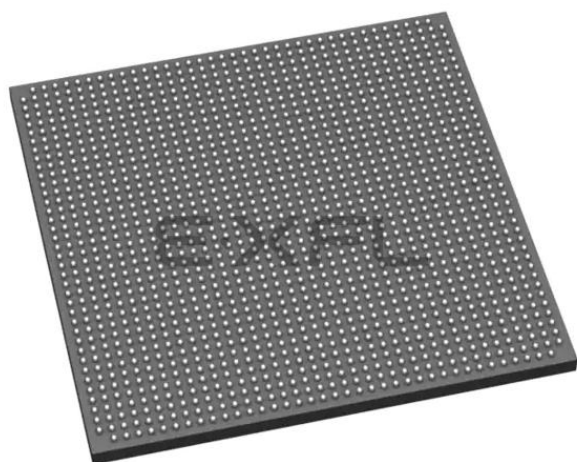




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™ -400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-1ffvb1517i

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 10: Power-on Current by Device⁽¹⁾

I_{CC} Min =	I_{CCQ} +	XCZU2	XCZU3	XCZU4	XCZU5	XCZU6	XCZU7	XCZU9	XCZU11	XCZU15	XCZU17	XCZU19	Units
$I_{CCINTMIN}$	I_{CCINTQ}^+	464	464	770	770	1800	1514	1800	1961	2242	3433	3433	mA
$I_{CCINT_IOMIN}^+$ $I_{CCBRAMMIN}$	$I_{CCBRAMQ}^+$ $I_{CCINT_IOQ}^+$	155	155	257	257	600	505	600	654	748	1145	1145	mA
I_{CCOMIN}	I_{CCOQ}^+	50	50	50	50	50	50	50	55	63	96	96	mA
$I_{CCAUXMIN}^+$ I_{CCAUX_IOMIN}	I_{CCAUXQ}^+ $I_{CCAUX_IOQ}^+$	111	111	386	386	650	362	650	709	810	1240	1240	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

Table 11: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT} .	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO} .	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU} .	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO} .	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX} .	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM} .	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms
$T_{VCC_PSINTFP}$	Ramp time from GND to 95% of $V_{CC_PSINTFP}$.	0.2	40	ms
$T_{VCC_PSINTLP}$	Ramp time from GND to 95% of $V_{CC_PSINTLP}$.	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX} .	0.2	40	ms
$T_{VCC_PSINTFP_DDR}$	Ramp time from GND to 95% of $V_{CC_PSINTFP_DDR}$.	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC} .	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL} .	0.2	40	ms
$T_{PS_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC_MGTRAVCC}$.	0.2	40	ms
$T_{PS_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC_MGTRAVTT}$.	0.2	40	ms

PL I/O Levels

Table 14: SelectIO DC Input and Output Levels For HD I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	8.0	-8.0
HSTL_I_18	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	8.0	-8.0
HSUL_12	-0.300	V _{REF} - 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	Note 4	Note 4
LVC MOS15	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	Note 5	Note 5
LVC MOS18	-0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} - 0.450	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	V _{CCO} + 0.300	0.400	V _{CCO} - 0.400	Note 5	Note 5
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	V _{CCO} - 0.400	Note 5	Note 5
LVTTL	-0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	14.25	-14.25
SSTL135	-0.300	V _{REF} - 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	8.9	-8.9
SSTL135_II	-0.300	V _{REF} - 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 - 0.150	V _{CCO} /2 + 0.150	13.0	-13.0
SSTL15	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.175	V _{CCO} /2 + 0.175	8.9	-8.9
SSTL15_II	-0.300	V _{REF} - 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 - 0.175	V _{CCO} /2 + 0.175	13.0	-13.0
SSTL18_I	-0.300	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 - 0.470	V _{CCO} /2 + 0.470	8.0	-8.0
SSTL18_II	-0.300	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 - 0.600	V _{CCO} /2 + 0.600	13.4	-13.4
MIPI_DPHY_DCI_LP ⁽⁶⁾	-0.300	0.550	0.880	V _{CCO} + 0.300	0.050	1.100	0.01	-0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 16](#), [Table 20](#), [Table 21](#), and [Table 22](#).
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 15: SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	5.8	−5.8
HSTL_I_12	−0.300	V _{REF} − 0.080	V _{REF} + 0.080	V _{CCO} + 0.300	25% V _{CCO}	75% V _{CCO}	4.1	−4.1
HSTL_I_18	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	6.2	−6.2
HSUL_12	−0.300	V _{REF} − 0.130	V _{REF} + 0.130	V _{CCO} + 0.300	20% V _{CCO}	80% V _{CCO}	0.1	−0.1
LVC MOS12	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.400	V _{CCO} − 0.400	Note 4	Note 4
LVC MOS15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVC MOS18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	Note 5	Note 5
LVDCI_15	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
LVDCI_18	−0.300	35% V _{CCO}	65% V _{CCO}	V _{CCO} + 0.300	0.450	V _{CCO} − 0.450	7.0	−7.0
SSTL12	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	8.0	−8.0
SSTL135	−0.300	V _{REF} − 0.090	V _{REF} + 0.090	V _{CCO} + 0.300	V _{CCO} /2 − 0.150	V _{CCO} /2 + 0.150	9.0	−9.0
SSTL15	−0.300	V _{REF} − 0.100	V _{REF} + 0.100	V _{CCO} + 0.300	V _{CCO} /2 − 0.175	V _{CCO} /2 + 0.175	10.0	−10.0
SSTL18_I	−0.300	V _{REF} − 0.125	V _{REF} + 0.125	V _{CCO} + 0.300	V _{CCO} /2 − 0.470	V _{CCO} /2 + 0.470	7.0	−7.0
MIPI_DPHY_DCI_LP ⁽⁶⁾	−0.300	0.550	0.880	V _{CCO} + 0.300	0.050	1.100	0.01	−0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 16](#), [Table 20](#), [Table 21](#), and [Table 22](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: DC Input Levels for Single-ended POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V _{IL}		V _{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300
POD12	−0.300	V _{REF} − 0.068	V _{REF} + 0.068	V _{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 23: LVDS_25 DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	100	350	600 ⁽²⁾	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 24: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		1.710	1.800	1.890	V
$V_{ODIFF}^{(2)}$	Differential output voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
$V_{OCM}^{(2)}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
$V_{IDIFF}^{(3)}$	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$		100	350	600 ⁽³⁾	mV
$V_{ICM_DC}^{(4)}$	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
$V_{ICM_AC}^{(5)}$	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 25](#).

Table 25: Speed Specification Version By Device

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Table 30: PS DDR Performance (Cont'd)

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR3	All FFV packages, FBVB900 and SFVC784	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SFVA625	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1333	664	1333	664	1333	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
DDR3L	All FFV packages, FBVB900 and SFVC784	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single rank component	664	1600	664	1600	664	1600	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1333	664	1333	664	1333	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR3	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁶⁾	664	1600	664	1600	664	1600	Mb/s
		Dual die package ⁽⁶⁾	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single die package ⁽⁶⁾	664	1333	664	1333	664	1333	Mb/s
		Dual die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
2. Includes: 1 rank 1 slot, dual-die package 2 rank.
3. Includes: 2 rank 1 slot.
4. Dual die package includes single die with ECC.
5. LPDDR4 support is only available as a 32-bit interface.
6. 64-bit LPDDR3 interface performance values are defined without ECC support.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	—	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	—	16.5	MHz
$T_{TTCICLK}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$T_{TTCICLK}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	—	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	—	100	MHz

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3 (1)	-2 (1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces (Cont'd)

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	800	800	800	800	606	Mb/s
QDR II +	All	Single rank component ⁽⁷⁾	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF_DELAY_PAD_I}}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF_DELAY_O_PAD}}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I / O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVC MOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVC MOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVC MOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVC MOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVC MOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVC MOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVC MOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVC MOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVC MOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVC MOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVC MOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVC MOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVC MOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVC MOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVC MOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVC MOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVC MOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVC MOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVC MOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVC MOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVC MOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVC MOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVC MOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVC MOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVC MOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVC MOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVC MOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVC MOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVC MOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVC MOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVC MOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of T_{OUTBUF_DELAY_TE_PAD} and T_{INBUF_DELAY_IBUFDIS_O}. T_{OUTBUF_DELAY_TE_PAD} is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{INBUF_DELAY_IBUFDIS_O} is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the INTERMDISABLE pin is used.

Table 77: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V		0.85V		0.72V	
		-3	-2	-1	-2	-1	
T _{OUTBUF_DELAY_TE_PAD}	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
T _{INBUF_DELAY_IBUFDIS_O}	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

Table 78: Input Delay Measurement Methodology (Cont'd)

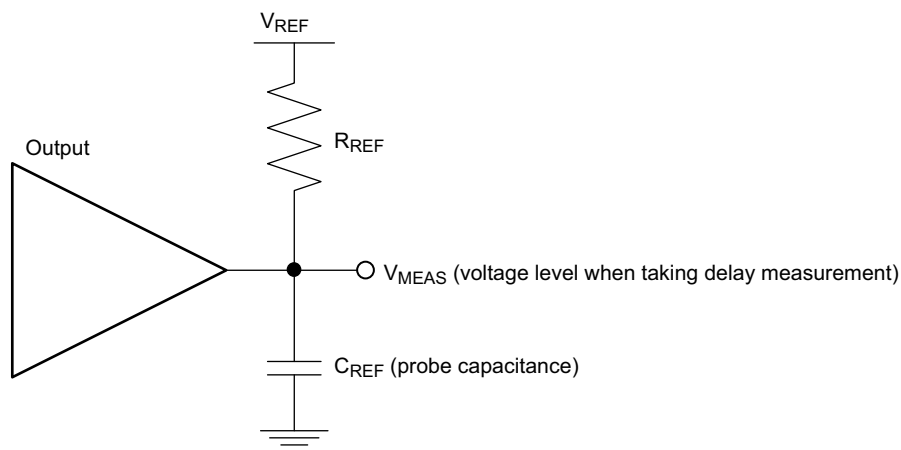
Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0 ⁽⁶⁾	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

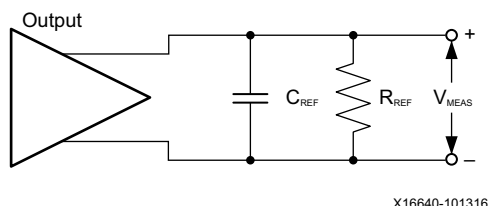
Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-101316

Figure 1: Single-Ended Test Setup



X16640-101316

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 79](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoC that include this memory.

Table 81: UltraRAM Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	481	MHz
F _{MAX_ECC}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	315	MHz
F _{MAX_NORPIPELINE}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	408	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	650	700	730	800	832	ps
T _{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle					

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{REFCLK}	REFCLK frequency for IDELAYCTRL (component mode).	300 to 800					MHz
	REFCLK frequency for BITSlice_CONTROL (native mode). ⁽¹⁾	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	300 to 2133	MHz
T _{MINPER_CLK}	Minimum period for IODELAY clock.	3.195	3.195	3.195	3.195	3.195	ns
T _{MINPER_RST}	Minimum reset pulse width.	52.00					ns
T _{IDELAY_RESOLUTION} / T _{ODELAY_RESOLUTION}	IDELAY/ODELAY chain resolution.	2.1 to 12					ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

[Table 94](#) summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 94: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage.	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽³⁾		–	100	–	nF

Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
- V_{RX_TERM} is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 97: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375 ⁽¹⁾		16.375 ⁽¹⁾		12.5		12.5		10.3125		Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽²⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽³⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽⁴⁾ .	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

- GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
- The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
- The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
- The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 98: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.	250	MHz

Table 105: GTH Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽¹⁾	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽²⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽²⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI ⁽²⁾	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort ⁽²⁾	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PH-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

PL SYSMON I2C/PMBus Interfaces

Table 125: PL SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 126: PL SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1 . Updated Table 2 , Table 4 , Table 6 , Table 7 , and Table 9 . Revised the Power Supply Sequencing section including Table 10 . Added PS and VCU ramp times to Table 11 . Revised V_{ODIFF} in Table 24 . Updated Table 25 . Added Note 1 to Table 26 . Table 30 replaces the previous three PS memory performance tables. Added values to Table 34 , Table 37 , and Table 38 . Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40 . Added Note 3 to Table 41 . Added Note 3 to Table 42 . Added Note 1 to Table 45 . Updated Table 48 and removed Note 3 . Added data to Table 56 . Updated Table 60 . Added Table 61 . Updated Table 63 . Revised Table 69 . Added data to Table 70 . Added Note 2 to Table 71 . Updated Table 74 and added Note 4 . Updated V_L and V_H values in Table 78 . Added T_{MINPER_CLK} , revised F_{REFCLK} , and Note 1 to Table 82 . Added $MMCM_F_{DPRCLK_MAX}$ to Table 85 and $PLL_F_{DPRCLK_MAX}$ to Table 86 . Added data to Table 94 , Table 96 , Table 98 , Table 101 , and updated the note references in Table 102 . Updated Table 103 and added Note 8 . Updated Table 104 and added Note 7 . Added more protocols, Note 1 and Note 2 to Table 105 . Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 105 . Added Note 1 to Table 109 . Added data to Table 106 , Table 108 , Table 110 , Table 113 . Added Note 2 to Table 112 . Added note references in Table 114 . Updated Table 115 and added Note 8 . Updated Table 116 and added Note 7 . Added more protocols and Note 3 to Table 117 . Removed the GTy Transceiver Protocol Jitter Characteristics section because it is covered in Table 117 . Revised Table 124 . Added T_{POR} and updated F_{ICAPCK} in Table 127 . Updated the Automotive Applications Disclaimer .
06/20/2016	1.1	Updated the Summary description. In Table 1 , revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU} , I_{RPD} , and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5 . Updated Note 5 in Table 4 . Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added $MIPI_DPHY_DCI$ to Table 14 , Table 15 , and Table 17 . Updated Table 23 , including removing the V_{CCO} specification and adding Note 1 . Added Note 1 to Table 24 . Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28 . Updated the -2 value in Table 29 . Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33 . Added VCO frequencies to Table 36 . Added the T_{PSPOR} minimum to Table 37 and updated Note 1 . Added Table 38 . Added value delineation over V_{CCINT} operating voltages in Table 39 . Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42 . Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43 . Added $F_{TSI_REF_CLK}$ to Table 44 and updated Note 1 . In Table 45 , revised $T_{DCSDHCLK1}$, $T_{DCSDHCLK2}$, and $T_{DCSDHCLK3}$ and Note 1 . In Table 46 , revised Note 1 . In Table 47 , revised Note 1 . Revised Table 48 , including Note 1 , and added Note 2 and Note 3 . In Table 49 , Table 50 , Table 51 , and Table 53 , revised Note 1 . Updated Table 71 . Replaced Table 74 . Updated Table 75 and Table 76 . Updated Table 78 and Table 79 . In Table 80 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95 . Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97 . Added Table 100 and Table 112 . Added Note 2 to Table 106 . Revised data in Table 109 . Revised Table 114 . Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121 . Moved Table 123 . Revised INL in Table 124 . Added notes to Table 125 and Table 126 . In the eFUSE and Programming Conditions table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.