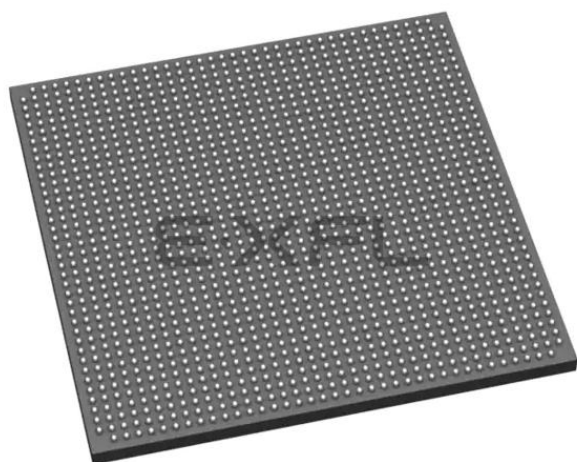




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-2ffvb1517e

Table 4: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
I_{CC_PSBATT} ⁽⁴⁾⁽⁵⁾	Battery supply current at $V_{CC_PSBATT} = 1.50V$, RTC enabled.	–	–	3650	nA
	Battery supply current at $V_{CC_PSBATT} = 1.50V$, RTC disabled.	–	–	650	nA
	Battery supply current at $V_{CC_PSBATT} = 1.20V$, RTC enabled.	–	–	3150	nA
	Battery supply current at $V_{CC_PSBATT} = 1.20V$, RTC disabled.	–	–	150	nA
I_{PSFS} ⁽⁶⁾	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
<i>Calibrated programmable on-die termination (DCI) in HP I/O banks⁽⁸⁾ (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{40}$.	–10% ⁽⁷⁾	40	+10% ⁽⁷⁾	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–10% ⁽⁷⁾	48	+10% ⁽⁷⁾	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{60}$.	–10% ⁽⁷⁾	60	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{40}$.	–10% ⁽⁷⁾	40	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{48}$.	–10% ⁽⁷⁾	48	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{60}$.	–10% ⁽⁷⁾	60	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{120}$.	–10% ⁽⁷⁾	120	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{240}$.	–10% ⁽⁷⁾	240	+10% ⁽⁷⁾	Ω
<i>Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{40}$.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{60}$.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{40}$.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{60}$.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{120}$.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{240}$.	–50%	240	+50%	Ω
<i>Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	$V_{CCO} \times 0.49$	$V_{CCO} \times 0.50$	$V_{CCO} \times 0.51$	V
	70% V_{CCO}	$V_{CCO} \times 0.69$	$V_{CCO} \times 0.70$	$V_{CCO} \times 0.71$	V

Table 11: Power Supply Ramp Time (Cont'd)

Symbol	Description	Min	Max	Units
$T_{V_{CCO_PSDDR}}$	Ramp time from GND to 95% of V_{CCO_PSDDR} .	0.2	40	ms
$T_{V_{CC_PSDDR_PLL}}$	Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$.	0.2	40	ms
$T_{V_{CCO_PSIO}}$	Ramp time from GND to 95% of V_{CCO_PSIO} .	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels⁽¹⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS33	-0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	-12
LVC MOS25	-0.300	0.700	1.700	$V_{CCO_PSIO} + 0.30$	0.70	1.70	12	-12
LVC MOS18	-0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	$V_{CCO_PSIO} + 0.30$	0.45	$V_{CCO_PSIO} - 0.45$	12	-12

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels⁽¹⁾

DDR Standard	V_{IL}		V_{IH}		$V_{OL}^{(2)}$	$V_{OH}^{(2)}$	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.8 \times V_{CCO_PSDDR} - 0.150$	$0.8 \times V_{CCO_PSDDR} + 0.150$	10	-0.1
LPDDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.3 \times V_{CCO_PSDDR} - 0.150$	$0.3 \times V_{CCO_PSDDR} + 0.150$	0.1	-10
DDR3	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.175$	$0.5 \times V_{CCO_PSDDR} + 0.175$	8	-8
LPDDR3	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8
DDR3L	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: Generic Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK1}	Quad-SPI clock duty cycle.	15 pF	45	55	%
T _{QSPISSSCLK1}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
T _{QSPISCLKSS1}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
T _{QSPICKO1}	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
T _{QSPIDCK1}	Setup time, all inputs.	15 pF	0.9	–	ns
T _{QSPICKD1}	Hold time, all inputs.	15 pF	1.0	–	ns
F _{QSPICLK1}	Quad-SPI device clock frequency.	15 pF	–	150	MHz
F _{QSPIREFCLK1}	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK2}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSSCLK2}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS2}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO2}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK2}	Setup time, all inputs.	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
T _{QSPICKD2}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPICLK2}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
F _{QSPIREFCLK2}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.

PS eMMC Standard Interface

Table 46: eMMC Standard Interface⁽¹⁾

Symbol	Description	Min	Max	Units
eMMC Standard Interface				
T _{DCEMMCHSCLK}	eMMC clock duty cycle.	45	55	%
T _{EMMCHSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T _{EMMCHSDCK}	Input setup time, all inputs.	2.0	–	ns
T _{EMMCHSCKD}	Input hold time, all inputs.	2.0	–	ns
F _{EMMCHSCLK}	eMMC clock frequency.	–	25	MHz
eMMC High-Speed SDR Interface				
T _{DCEMMCHSCLK}	eMMC high-speed SDR clock duty cycle.	45	55	%
T _{EMMCHSCKO}	Clock to output delay, all outputs. ⁽²⁾	3.2	16.8	ns
T _{EMMCHSDIVW}	Input valid data window. ⁽³⁾	0.4	–	UI
F _{EMMCHSCLK}	eMMC high speed SDR clock frequency.	–	50	MHz
eMMC High-Speed DDR Interface				
T _{DCEMMCDDRCLK}	eMMC high-speed DDR clock duty cycle.	45	55	%
T _{EMMCDDRCKO1}	Data clock to output delay. ⁽²⁾	2.7	7.3	ns
T _{EMMCSDR1VW}	Input valid data window. ⁽³⁾	3.5	–	ns
T _{EMMCDDRCKO2}	Command clock to output delay.	3.2	16	ns
T _{EMMCDDRCK2}	Command input setup time.	3.9	–	ns
T _{EMMCDDRCKD2}	Command input hold time.	2.5	–	ns
F _{EMMCDDRCLK}	eMMC high-speed DDR clock frequency.	–	50	MHz
eMMC HS200 Interface				
T _{DCEMMCHS200CLK}	eMMC HS200 clock duty cycle.	40	60	%
T _{EMMCHS200CKO}	Clock to output delay, all outputs. ⁽²⁾	1.0	3.4	ns
T _{EMMCSDR1VW}	Input valid data window. ⁽³⁾	0.4	–	UI
F _{EMMCHS200CLK}	eMMC HS200 clock frequency.	–	200	MHz

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS I2C Controller Interface

Table 47: I2C Interface⁽¹⁾

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	μs
$T_{I2CFCKH}$	SCL High time.	0.6	–	μs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	μs
$T_{I2CSCKH}$	SCL High time.	4.0	–	μs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SPI Controller Interface

Table 48: SPI Interfaces⁽¹⁾

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two $F_{SPI_REF_CLK}$ delays are programmed between CS and CLK for $T_{MSPISSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: CAN Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	μs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	μs
$F_{CAN_REF_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 61: PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
PLL _{REFCLK} MASK	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

- For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: PS-GTR Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T _{RTX}	TX rise time.	20%–80%	–	65	–	ps
T _{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 63: PS-GTR Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX _{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: PCI Express Protocol Characteristics (PS-GTR Transceivers)⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2 ⁽²⁾	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: DisplayPort Protocol Characteristics (PS-GTR Transceivers)⁽¹⁾

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:

1. Only the transmitter is supported.

IOB High Performance (HP) Switching Characteristics

Table 76: IOB High Performance (HP) Switching Characteristics

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVC MOS18_F_8	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.600	0.573	0.600	0.733	0.733	0.767	0.733	0.767	ns
LVC MOS18_M_12	0.418	0.418	0.445	0.418	0.445	0.640	0.640	0.678	0.640	0.678	0.670	0.670	0.709	0.670	0.709	ns
LVC MOS18_M_2	0.418	0.418	0.445	0.418	0.445	0.798	0.798	0.822	0.798	0.822	0.991	0.991	1.016	0.991	1.016	ns
LVC MOS18_M_4	0.418	0.418	0.445	0.418	0.445	0.664	0.664	0.693	0.664	0.693	0.798	0.798	0.836	0.798	0.836	ns
LVC MOS18_M_6	0.418	0.418	0.445	0.418	0.445	0.629	0.629	0.663	0.629	0.663	0.735	0.735	0.775	0.735	0.775	ns
LVC MOS18_M_8	0.418	0.418	0.445	0.418	0.445	0.626	0.626	0.661	0.626	0.661	0.705	0.705	0.746	0.705	0.746	ns
LVC MOS18_S_12	0.418	0.418	0.445	0.418	0.445	0.795	0.795	0.861	0.795	0.861	0.683	0.683	0.721	0.683	0.721	ns
LVC MOS18_S_2	0.418	0.418	0.445	0.418	0.445	0.862	0.862	0.897	0.862	0.897	1.076	1.076	1.098	1.076	1.098	ns
LVC MOS18_S_4	0.418	0.418	0.445	0.418	0.445	0.716	0.716	0.758	0.716	0.758	0.829	0.829	0.872	0.829	0.872	ns
LVC MOS18_S_6	0.418	0.418	0.445	0.418	0.445	0.682	0.682	0.724	0.682	0.724	0.724	0.724	0.762	0.724	0.762	ns
LVC MOS18_S_8	0.418	0.418	0.445	0.418	0.445	0.707	0.707	0.760	0.707	0.760	0.709	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.462	0.426	0.426	0.443	0.426	0.443	0.548	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.462	0.553	0.553	0.582	0.553	0.582	0.645	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.462	0.749	0.749	0.803	0.749	0.803	0.821	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.447	0.441	0.441	0.459	0.441	0.459	0.560	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.447	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.447	0.760	0.760	0.818	0.760	0.818	0.837	0.837	0.899	0.837	0.899	ns
LVDS	0.539	0.539	0.620	0.539	0.620	0.626	0.626	0.662	0.626	0.662	960.447	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.415	0.502	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	8.792	0.914	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.407	0.430	0.407	0.430	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.407	0.430	0.407	0.430	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.407	0.430	0.407	0.430	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.409	0.431	0.409	0.431	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.431	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.431	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.409	0.431	0.409	0.431	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.409	0.431	0.409	0.431	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.409	0.431	0.409	0.431	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.399	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.399	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.399	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of T_{OUTBUF_DELAY_TE_PAD} and T_{INBUF_DELAY_IBUFDIS_O}. T_{OUTBUF_DELAY_TE_PAD} is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{INBUF_DELAY_IBUFDIS_O} is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the INTERMDISABLE pin is used.

Table 77: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V		0.85V		0.72V	
		-3	-2	-1	-2	-1	
T _{OUTBUF_DELAY_TE_PAD}	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
T _{INBUF_DELAY_IBUFDIS_O}	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Table 88: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.								
T _{ICKOF_FAR}	Global clock input and output flip-flop <i>without</i> MMCM (far clock region).	XCZU2	N/A	5.27	5.68	5.80	6.13	ns
		XCZU3	N/A	5.27	5.68	5.80	6.13	ns
		XCZU4	5.07	6.06	6.61	6.23	7.10	ns
		XCZU5	5.07	6.06	6.61	6.23	7.10	ns
		XCZU6	5.38	6.49	6.97	7.14	7.59	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.38	6.49	6.97	7.14	7.59	ns
		XCZU11	6.18	7.41	8.11	7.66	8.99	ns
		XCZU15	5.38	6.49	6.96	7.19	7.71	ns
		XCZU17	6.21	7.53	8.07	8.36	8.90	ns
		XCZU19	6.21	7.53	8.07	8.36	8.90	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
T _{ICKOFMMCMCC}	Global clock input and output flip-flop <i>with</i> MMCM.	XCZU2	N/A	2.22	2.43	2.96	2.94	ns
		XCZU3	N/A	2.22	2.43	2.96	2.94	ns
		XCZU4	2.47	2.47	2.78	3.04	3.35	ns
		XCZU5	2.47	2.47	2.78	3.04	3.35	ns
		XCZU6	2.15	2.15	2.36	2.86	2.86	ns
		XCZU7	2.32	2.32	2.57	3.06	3.13	ns
		XCZU9	2.15	2.15	2.36	2.86	2.86	ns
		XCZU11	2.64	2.64	2.96	3.25	3.55	ns
		XCZU15	2.18	2.18	2.38	2.88	2.90	ns
		XCZU17	2.44	2.44	2.66	3.19	3.17	ns
XCZU19	2.44	2.44	2.66	3.19	3.17	ns		

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 90](#) and [Table 91](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T _{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU2}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU3}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU4}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU5}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU6}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T _{PHFD_ZU7}		Hold		−0.40	−0.40	−0.40	−0.21	−0.21	ns
T _{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU9}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU11}		Hold		−0.29	−0.29	−0.29	−0.09	0.19	ns
T _{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T _{PHFD_ZU15}		Hold		−0.04	−0.04	−0.04	0.27	0.43	ns
T _{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T _{PHFD_ZU17}		Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns
T _{PSFD_ZU19}	Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns	
T _{PHFD_ZU19}	Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 91: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T _{PSMMCMCC_ZU2}	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU2}		Hold			−0.19	−0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU3}		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU3}		Hold			−0.19	−0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU4}		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU4}		Hold		−0.12	−0.12	−0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU5}		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU5}		Hold		−0.12	−0.12	−0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU6}		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU6}		Hold		−0.11	−0.11	−0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU7}		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
T _{PHMMCMCC_ZU7}		Hold		−0.14	−0.14	−0.14	0.37	0.38	ns
T _{PSMMCMCC_ZU9}		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU9}		Hold		−0.11	−0.11	−0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU11}		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
T _{PHMMCMCC_ZU11}		Hold		−0.08	−0.08	0.04	0.35	0.74	ns
T _{PSMMCMCC_ZU15}		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU15}		Hold		−0.10	−0.10	−0.10	0.17	0.19	ns
T _{PSMMCMCC_ZU17}		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
T _{PHMMCMCC_ZU17}		Hold		−0.16	−0.16	−0.16	0.31	0.34	ns
T _{PSMMCMCC_ZU19}	Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns	
T _{PHMMCMCC_ZU19}	Hold		−0.16	−0.16	−0.16	0.31	0.34	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 103: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

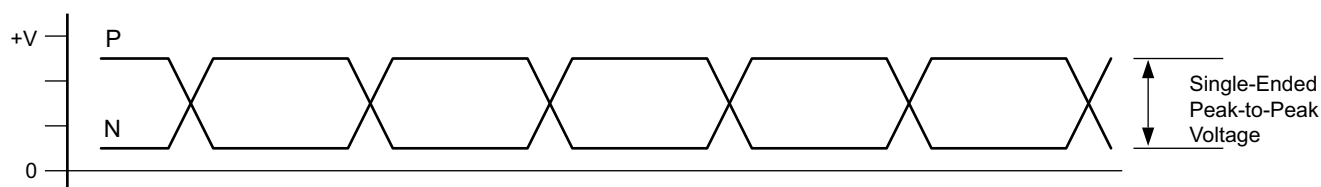
Symbol	Description	Condition	Min	Typ	Max	Units
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

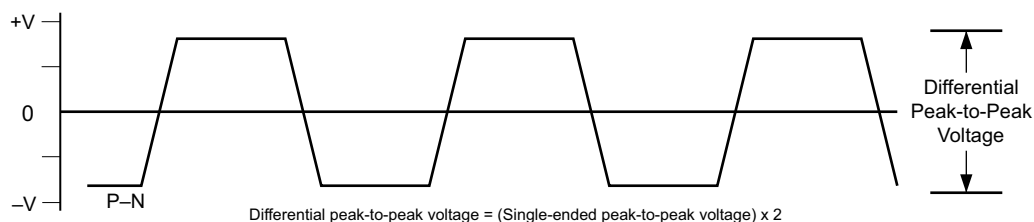
Table 104: GTH Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTHRX}	Serial data rate		0.500	–	F _{GTHMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	



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Figure 5: Single-Ended Peak-to-Peak Voltage



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Figure 6: Differential Peak-to-Peak Voltage

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 107: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

Table 113: GTY Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock.		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10 ⁶	UI

Table 114: GTY Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA		511.719	511.719	402.833	402.833	322.266	MHz	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK		511.719	511.719	511.719	511.719	511.719	MHz	
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI