Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-2ffvd1760e

Table 1: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{CCO_PSDDR}	PS DDR I/O supply voltage.	–0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	–0.500	2.000	V
V_{CCO_PSIO}	PS I/O supply.	–0.500	3.630	V
V_{PSIN}[2]	PS I/O input voltage.	–0.500	V_{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	–0.500	V_{CCO_PSDDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	–0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage.	–0.500	1.000	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks.	–0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	–0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	–0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	–0.500	2.000	V
V_{CCAUX_IO}[4]	Auxiliary supply voltage for the I/O banks.	–0.500	2.000	V
V_{REF}	Input reference voltage.	–0.500	2.000	V
V_{IN}[2][5][7]	I/O input voltage for HD I/O banks.[6]	–0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	–0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad.	–20	20	mA
I_{RMS}	Available RMS output current at the pad.	–20	20	mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.[8]	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.[9]	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.[10]	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–	6	mA

PL I/O Levels

Table 14: **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU2EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU4CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

PS eMMC Standard Interface

Table 46: **eMMC Standard Interface(1)**

Symbol	Description	Min	Max	Units
eMMC Standard Interface				
$T_{DCEMMCHSCLK}$	eMMC clock duty cycle.	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs.	–2.0	4.5	ns
$T_{EMMCHSDCK}$	Input setup time, all inputs.	2.0	–	ns
$T_{EMMCHSCKD}$	Input hold time, all inputs.	2.0	–	ns
$F_{EMMCHSCLK}$	eMMC clock frequency.	–	25	MHz
eMMC High-Speed SDR Interface				
$T_{DCEMMCHSCLK}$	eMMC high-speed SDR clock duty cycle.	45	55	%
$T_{EMMCHSCKO}$	Clock to output delay, all outputs.(2)	3.2	16.8	ns
$T_{EMMCHSDIVW}$	Input valid data window.(3)	0.4	–	UI
$F_{EMMCHSCLK}$	eMMC high speed SDR clock frequency.	–	50	MHz
eMMC High-Speed DDR Interface				
$T_{DCEMMCDDRCLK}$	eMMC high-speed DDR clock duty cycle.	45	55	%
$T_{EMMCDDRSCKO1}$	Data clock to output delay.(2)	2.7	7.3	ns
$T_{EMMCSDRIVW}$	Input valid data window.(3)	3.5	–	ns
$T_{EMMCDDRSCKO2}$	Command clock to output delay.	3.2	16	ns
$T_{EMMCDDRDCK2}$	Command input setup time.	3.9	–	ns
$T_{EMMCDDRCKD2}$	Command input hold time.	2.5	–	ns
$F_{EMMCDDRCLK}$	eMMC high-speed DDR clock frequency.	–	50	MHz
eMMC HS200 Interface				
$T_{DCEMMCHS200CLK}$	eMMC HS200 clock duty cycle.	40	60	%
$T_{EMMCHS200CKO}$	Clock to output delay, all outputs.(2)	1.0	3.4	ns
$T_{EMMCSDR1IVW}$	Input valid data window.(3)	0.4	–	UI
$F_{EMMCHS200CLK}$	eMMC HS200 clock frequency.	–	200	MHz

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

Table 63: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX_{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: **PCI Express Protocol Characteristics (PS-GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:
1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: **DisplayPort Protocol Characteristics (PS-GTR Transceivers)(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:
1. Only the transmitter is supported.

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 22. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3(3)		-2(3)		-1		-2(3)		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(4)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(4)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS18_F_8	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.600	0.573	0.600	0.733	0.733	0.767	0.733	0.767	ns
LVCMOS18_M_12	0.418	0.418	0.445	0.418	0.445	0.640	0.640	0.678	0.640	0.678	0.670	0.670	0.709	0.670	0.709	ns
LVCMOS18_M_2	0.418	0.418	0.445	0.418	0.445	0.798	0.798	0.822	0.798	0.822	0.991	0.991	1.016	0.991	1.016	ns
LVCMOS18_M_4	0.418	0.418	0.445	0.418	0.445	0.664	0.664	0.693	0.664	0.693	0.798	0.798	0.836	0.798	0.836	ns
LVCMOS18_M_6	0.418	0.418	0.445	0.418	0.445	0.629	0.629	0.663	0.629	0.663	0.735	0.735	0.775	0.735	0.775	ns
LVCMOS18_M_8	0.418	0.418	0.445	0.418	0.445	0.626	0.626	0.661	0.626	0.661	0.705	0.705	0.746	0.705	0.746	ns
LVCMOS18_S_12	0.418	0.418	0.445	0.418	0.445	0.795	0.795	0.861	0.795	0.861	0.683	0.683	0.721	0.683	0.721	ns
LVCMOS18_S_2	0.418	0.418	0.445	0.418	0.445	0.862	0.862	0.897	0.862	0.897	1.076	1.076	1.098	1.076	1.098	ns
LVCMOS18_S_4	0.418	0.418	0.445	0.418	0.445	0.716	0.716	0.758	0.716	0.758	0.829	0.829	0.872	0.829	0.872	ns
LVCMOS18_S_6	0.418	0.418	0.445	0.418	0.445	0.682	0.682	0.724	0.682	0.724	0.724	0.724	0.762	0.724	0.762	ns
LVCMOS18_S_8	0.418	0.418	0.445	0.418	0.445	0.707	0.707	0.760	0.707	0.760	0.709	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.462	0.426	0.426	0.443	0.426	0.443	0.548	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.462	0.553	0.553	0.582	0.553	0.582	0.645	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.462	0.749	0.749	0.803	0.749	0.803	0.821	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.447	0.441	0.441	0.459	0.441	0.459	0.560	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.447	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.447	0.760	0.760	0.818	0.760	0.818	0.837	0.837	0.899	0.837	0.899	ns
LVDS	0.539	0.539	0.620	0.539	0.620	0.626	0.626	0.662	0.626	0.662	960.447	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.415	0.502	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	8.792	0.914	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.407	0.430	0.407	0.430	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.407	0.430	0.407	0.430	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.407	0.430	0.407	0.430	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.409	0.431	0.409	0.431	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.431	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.431	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.409	0.431	0.409	0.431	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.409	0.431	0.409	0.431	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.409	0.431	0.409	0.431	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.399	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.399	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.399	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0 (6)	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0 (6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0 (6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0 (6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0 (6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0 (6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0 (6)	–
LVDS_25, 2.5V	LVDS_25	1.25 – 0.125	1.25 + 0.125	0 (6)	–

Table 78: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Block RAM and FIFO Switching Characteristics

Table 80: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T_{PW}[(1)]	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 87 through Table 89 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.								
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
		XCZU19	5.72	6.90	7.40	7.62	8.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T_{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU2}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU3}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU4}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU5}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU6}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T_{PHFD_ZU7}		Hold		–0.40	–0.40	–0.40	–0.21	–0.21	ns
T_{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU9}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU11}		Hold		–0.29	–0.29	–0.29	–0.09	0.19	ns
T_{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T_{PHFD_ZU15}		Hold		–0.04	–0.04	–0.04	0.27	0.43	ns
T_{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU17}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns
T_{PSFD_ZU19}		Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU19}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
$T_{PSMMCMCC\_ZU2}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU2}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU3}$		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU3}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU4}$		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU4}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU5}$		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU5}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU6}$		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU6}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU7}$		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
$T_{PHMMCMCC\_ZU7}$		Hold		–0.14	–0.14	–0.14	0.37	0.38	ns
$T_{PSMMCMCC\_ZU9}$		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU9}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU11}$		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
$T_{PHMMCMCC\_ZU11}$		Hold		–0.08	–0.08	0.04	0.35	0.74	ns
$T_{PSMMCMCC\_ZU15}$		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU15}$		Hold		–0.10	–0.10	–0.10	0.17	0.19	ns
$T_{PSMMCMCC\_ZU17}$		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU17}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns
$T_{PSMMCMCC\_ZU19}$		Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU19}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 92: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T_{SAMP_BUFG} (1)	510	610	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	150	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	110	ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 93: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCZU2	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU3	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU4	SFVC784		ps
			FBVB900		ps
		XCZU5	SFVC784		ps
			FBVB900		ps
		XCZU6	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU7	FBVB900	141	ps
			FFVC1156	175	ps
			FFVF1517	305	ps
		XCZU9	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU11	FFVC1156		ps
			FFVB1517		ps
			FFVF1517		ps
			FFVC1760	215	ps
		XCZU15	FFVC900	118	ps
			FFVB1156	132	ps
		XCZU17	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps
		XCZU19	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 102: **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

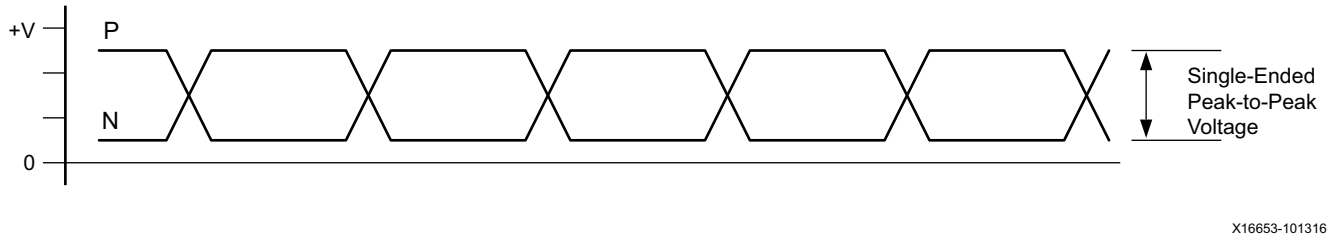

Figure 5: **Single-Ended Peak-to-Peak Voltage**

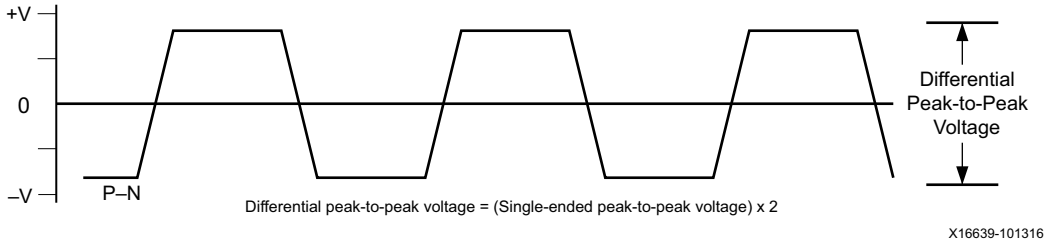

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.