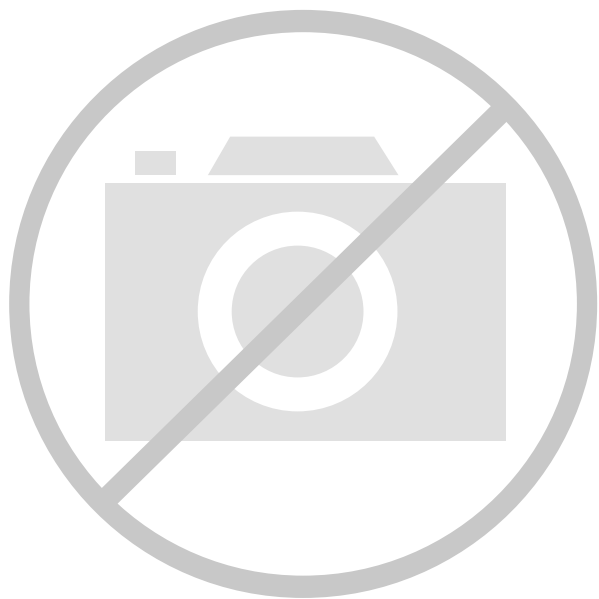




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1924-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-2ffve1924e

Available Speed Grades and Operating Voltages

Table 3 describes the speed grades per device and the V_{CCINT} operating supply voltages for the full-power, low-power, and DDR domains. For more information on selecting devices and speed grades, see the *UltraScale Architecture and Product Overview* (DS890).

Table 3: Available Speed Grades and Operating Voltages

Speed Grade	V_{CCINT}	$V_{CC_PSINTLP}$	$V_{CC_PSINTFP}$	$V_{CC_PSINTFP_DDR}$	Units
-3E	0.90	0.90	0.90	0.90	V
-2E	0.85	0.85	0.85	0.85	V
-2I	0.85	0.85	0.85	0.85	V
-2LE	0.85	0.85	0.85	0.85	V
-1E	0.85	0.85	0.85	0.85	V
-1I	0.85	0.85	0.85	0.85	V
-1LI	0.85	0.85	0.85	0.85	V
-2LE	0.72	0.85	0.85	0.85	V
-1LI	0.72	0.85	0.85	0.85	V

DC Characteristics Over Recommended Operating Conditions

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	μ A
I_L	Input or output leakage current per pin (sample-tested). ⁽²⁾	–	–	15	μ A
C_{IN} ⁽³⁾	Die input capacitance at the pad (HP I/O).	–	–	3.1	pF
	Die input capacitance at the pad (HD I/O).	–	–	4.75	pF
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 3.3V$.	75	–	190	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 2.5V$.	50	–	169	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.8V$.	60	–	120	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.5V$.	30	–	120	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO} = 1.2V$.	10	–	100	μ A
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$.	60	–	200	μ A
	Pad pull-down (when selected) at $V_{IN} = 1.8V$.	29	–	120	μ A
$I_{CCADCONPL}$	Analog supply current for the PL SYSMON circuits in the power-up state.	–	–	8	mA
$I_{CCADCONPS}$	Analog supply current for the PS SYSMON circuits in the power-up state.	–	–	10	mA
$I_{CCADCOFFPL}$	Analog supply current for the PL SYSMON circuits in the power-down state.	–	–	1.5	mA
$I_{CCADCOFFPS}$	Analog supply current for the PS SYSMON circuits in the power-down state.	–	–	1.8	mA

Table 4: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA .
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
- If VRP resides at a different bank (DCI cascade), the range increases to $\pm 15\%$.
- VRP resistor tolerance is $(240\Omega \pm 1\%)$
- On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 5: PS MIO Pull-up and Pull-down Current

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 3.3V$.	20	80	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 2.5V$.	20	80	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 1.8V$.	15	65	μA
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$.	20	80	μA
	Pad pull-down (when selected) at $V_{IN} = 2.5V$.	20	80	μA
	Pad pull-down (when selected) at $V_{IN} = 1.8V$.	15	65	μA

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 10: Power-on Current by Device⁽¹⁾

I_{CC} Min =	I_{CCQ} +	XCZU2	XCZU3	XCZU4	XCZU5	XCZU6	XCZU7	XCZU9	XCZU11	XCZU15	XCZU17	XCZU19	Units
$I_{CCINTMIN}$	I_{CCINTQ}^+	464	464	770	770	1800	1514	1800	1961	2242	3433	3433	mA
$I_{CCINT_IOMIN}^+$ $I_{CCBRAMMIN}$	$I_{CCBRAMQ}^+$ $I_{CCINT_IOQ}^+$	155	155	257	257	600	505	600	654	748	1145	1145	mA
I_{CCOMIN}	I_{CCOQ}^+	50	50	50	50	50	50	50	55	63	96	96	mA
$I_{CCAUXMIN}^+$ I_{CCAUX_IOMIN}	I_{CCAUXQ}^+ $I_{CCAUX_IOQ}^+$	111	111	386	386	650	362	650	709	810	1240	1240	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

Table 11: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT} .	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO} .	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU} .	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO} .	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX} .	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM} .	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms
$T_{VCC_PSINTFP}$	Ramp time from GND to 95% of $V_{CC_PSINTFP}$.	0.2	40	ms
$T_{VCC_PSINTLP}$	Ramp time from GND to 95% of $V_{CC_PSINTLP}$.	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX} .	0.2	40	ms
$T_{VCC_PSINTFP_DDR}$	Ramp time from GND to 95% of $V_{CC_PSINTFP_DDR}$.	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC} .	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL} .	0.2	40	ms
$T_{PS_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC_MGTRAVCC}$.	0.2	40	ms
$T_{PS_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC_MGTRAVTT}$.	0.2	40	ms

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU2EG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU3CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU3EG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU4CG	-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU4EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU4EV	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU5CG	-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release

Device	Speed Grade and V _{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCZU2CG	N/A	Vivado tools 2017.1 v1.10					
XCZU2EG	N/A	Vivado tools 2017.1 v1.10					
XCZU3CG	N/A	Vivado tools 2017.1 v1.10					
XCZU3EG	N/A	Vivado tools 2017.1 v1.10					
XCZU4CG	N/A						
XCZU4EG							
XCZU4EV							
XCZU5CG	N/A						
XCZU5EG							
XCZU5EV							
XCZU6CG	N/A	Vivado tools 2017.1 v1.10					
XCZU6EG		Vivado tools 2017.1 v1.10					
XCZU7CG	N/A						
XCZU7EG							
XCZU7EV							
XCZU9CG	N/A	Vivado tools 2017.1 v1.10					
XCZU9EG		Vivado tools 2017.1 v1.10					
XCZU11EG							
XCZU15EG							
XCZU17EG							
XCZU19EG							

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Processor System (PS) Performance Characteristics

Table 28: Processor Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F _{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F _{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: Configuration and Security Unit Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{CSUCIBMAX}	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: PS DDR Performance

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁵⁾	664	2400	664	2400	664	2400	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package ⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package ⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s

PS DAP Interface

Table 50: DAP Interface⁽¹⁾

Symbol	Description ⁽²⁾	Min	Max	Units
$T_{PDAPDCK}$	PS DAP input setup time.	3.0	–	ns
$T_{PDAPCKD}$	PS DAP input hold time.	2.0	–	ns
$T_{PDAPCKO}$	PS DAP clock to out delay.	–	10.86	ns
$T_{PDAPCLK}$	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: UART Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$BAUD_{TXMAX}$	Transmit baud rate.	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate.	–	6.25	Mb/s
$F_{UART_REF_CLK}$	UART reference clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: General Purpose I/O (GPIO) Interface

Symbol	Description	Min	Max	Units
$T_{PWGPIOH}$	Input High pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s
$T_{PWGPIOL}$	Input Low pulse width.	$10 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	μ s

PS Trace Interface

Table 53: Trace Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T_{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
$T_{DCTCECLK}$	Trace clock duty cycle.	45	55	%
F_{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	—	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	—	16.5	MHz
$T_{TTCICLKHL}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$T_{TTCICLKHL}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	—	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	—	100	MHz

PS-GTR Transceiver

Table 56: PS-GTR Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.		75	–	V _{PS_MGTRAVCC}	mV
V _{CMIN}	Common mode input voltage.		–	0	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to maximum value.	800	–	–	mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{PS_MGTRAVCC} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
R _{MGTREF}	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–	20	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽²⁾		–	100	–	nF

Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: PS-GTR Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R _{IN}	Differential input resistance.	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 58: PS-GTR Transceiver Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{GTRMAX}	PS-GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F _{GTRMIN}	PS-GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 59: PS-GTR Transceiver PLL/Lock Time Adaptation

Symbol	Description	Min	Typ	Max	Units
T _{LOCK}	Initial PLL lock.	–	–	0.11	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24 x 10 ⁶	UI

Table 67: USB 3.0 Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: Serial-GMII Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: PS SYSMON Specifications

Parameter	Comments	Conditions	Min	Typ	Max	Units
$V_{CC_PSADC} = 1.8V \pm 3\%$, $T_j = -40^\circ C$ to $100^\circ C$, typical values at $T_j = 40^\circ C$						
ADC Accuracy ($T_j = -55^\circ C$ to $125^\circ C$) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		$T_j = -55^\circ C$ to $110^\circ C$	–	–	± 3.5	$^\circ C$
		$T_j = 110^\circ C$ to $125^\circ C$	–	–	± 5	$^\circ C$
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 2.5	%

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF_DELAY_PAD_I}}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF_DELAY_O_PAD}}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I/O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, LVDCI, HSLVDCI, 1.5V	LVC MOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVC MOS, LVDCI, HSLVDCI, 1.8V	LVC MOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	$V_{REF} - 0.2875$	$V_{REF} + 0.2875$	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
POD10, 1.0V	POD10	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.7
POD12, 1.2V	POD12	$V_{REF} - 0.24$	$V_{REF} + 0.24$	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	$0.75 - 0.325$	$0.75 + 0.325$	0 ⁽⁶⁾	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	$0.9 - 0.4$	$0.9 + 0.4$	0 ⁽⁶⁾	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	$0.675 - 0.2875$	$0.675 + 0.2875$	0 ⁽⁶⁾	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	$0.75 - 0.325$	$0.75 + 0.325$	0 ⁽⁶⁾	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.4$	$0.9 + 0.4$	0 ⁽⁶⁾	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.5 - 0.2$	$0.5 + 0.2$	0 ⁽⁶⁾	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.6 - 0.25$	$0.6 + 0.25$	0 ⁽⁶⁾	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	$0.9 - 0.125$	$0.9 + 0.125$	0 ⁽⁶⁾	–
LVDS_25, 2.5V	LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁶⁾	–

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Table 104: GTH Transceiver Receiver Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10⁻¹².
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 105](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

[Table 106](#) and [Table 107](#) summarize the DC specifications of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 106: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 110: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTYDRPCLK}	GTYDRPCLK maximum frequency.	250	MHz

Table 111: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range.		60	–	820	MHz
T _{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask⁽¹⁾

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL _{REFCLKMASK}	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
CPLL _{REFCLKMASK}	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 117](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽²⁾	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽³⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽³⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: -2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: -2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: -2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: -2E, -2I, -1E, -1I Added -2E ($V_{CCINT} = 0.85V$) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{REFPCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the <i>PS NAND Memory Controller Interface</i> section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU_REF_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the <i>PS-GTR Transceiver</i> section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90, and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPP_OUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPP_OUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the <i>Integrated Interface Block for Interlaken</i> and <i>Integrated Interface Block for 100G Ethernet MAC and PCS</i> sections. Revised the <i>Configuration Switching Characteristics</i> section. Removed the <i>eFUSE Programming Conditions</i> table and added the specifications to Table 2 and Table 3.

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