AMD Xilinx - XCZU17EG-3FFVC1760E Datasheet

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz, 667MHz, 1.5GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-3ffvc1760e

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Quiescent Supply Current

Table 9: **Typical Quiescent Supply Current[(1)](2)(3)(4)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCZU2	N/A	393	393	344	344	mA
		XCZU3	N/A	393	393	344	344	mA
		XCZU4	719	684	684	601	601	mA
		XCZU5	719	684	684	601	601	mA
		XCZU6	1629	1549	1549	1358	1358	mA
		XCZU7	1263	1201	1201	1055	1055	mA
		XCZU9	1629	1549	1549	1358	1358	mA
		XCZU11	1786	1699	1699	1491	1491	mA
		XCZU15	1987	1890	1890	1660	1660	mA
		XCZU17	2728	2594	2594	2275	2275	mA
		XCZU19	2728	2594	2594	2275	2275	mA
I_{CCINT_IOQ}	Quiescent V_{CCINT_IO} supply current.	XCZU2	N/A	44	44	44	44	mA
		XCZU3	N/A	44	44	44	44	mA
		XCZU4	61	59	59	59	59	mA
		XCZU5	61	59	59	59	59	mA
		XCZU6	61	59	59	59	59	mA
		XCZU7	120	115	115	115	115	mA
		XCZU9	61	59	59	59	59	mA
		XCZU11	120	115	115	115	115	mA
		XCZU15	61	59	59	59	59	mA
		XCZU17	164	158	158	158	158	mA
		XCZU19	164	158	158	158	158	mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	All devices	1	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCZU2	N/A	55	55	55	55	mA
		XCZU3	N/A	55	55	55	55	mA
		XCZU4	90	90	90	90	90	mA
		XCZU5	90	90	90	90	90	mA
		XCZU6	227	227	227	227	227	mA
		XCZU7	174	174	174	174	174	mA
		XCZU9	227	227	227	227	227	mA
		XCZU11	255	255	255	255	255	mA
		XCZU15	266	266	266	266	266	mA
		XCZU17	396	396	396	396	396	mA
		XCZU19	396	396	396	396	396	mA

Table 11: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**(1)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:

1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**(1)

DDR Standard	V_{IL}		V_{IH}		V_{OL}(2)	V_{OH}(2)	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 17: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{ILHS}(3)	V_{IHHS}(3)	V_{OCM}(V)(4)			V_{OD}(V)(5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS(8)	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(9)	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage $(Q - \overline{Q})$.
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage $(Q - \overline{Q})$.
6. LVDS_25 is specified in Table 23.
7. LVDS is specified in Table 24.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Table 31: **PS NAND NV-DDR Synchronous Performance**

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
NV-DDR[1]	5	200	200	200	Mb/s
	4	166.6	166.6	166.6	Mb/s
	3	133.3	133.3	133.3	Mb/s
	2	100	100	100	Mb/s
	1	66.6	66.6	66.6	Mb/s
	0	40	40	40	Mb/s

Notes:

1. The PS NAND memory controller interface for NV-DDR switching characteristics meets the requirements of the ONFI 3.1 specification.

Table 32: **PS NAND SDR Asynchronous Performance**

Memory Standard	Mode	Speed Grade			Units
		-3	-2	-1	
		Max	Max	Max	
SDR(1)(2)	5	50	50	50	Mb/s
	4	40	40	40	Mb/s
	3	33.3	33.3	33.3	Mb/s
	2	28.5	28.5	28.5	Mb/s
	1	20	20	20	Mb/s
	0	10	10	10	Mb/s

Notes:

1. The PS NAND memory controller interface for SDR switching characteristics meets the requirements of the ONFI 3.1 specification.
2. The NAND controller reference clock frequency maximum is 83 MHz.

Table 33: **PS-PL Interface Performance**

Symbol	Description	Min	Max	Units
$F_{EMIOGEMCLK}$	EMIO gigabit Ethernet controller maximum frequency.	–	125	MHz
$F_{EMIOSDCLK}$	EMIO SD controller maximum frequency.	–	25	MHz
$F_{EMIOSPICLK}$	EMIO SPI controller maximum frequency.	–	25	MHz
$F_{EMIOTRACECLK}$	EMIO trace controller maximum frequency.	–	125	MHz
$F_{FCIDMACLK}$	Flow control interface DMA maximum frequency.	–	333	MHz
F_{AXICLK}	Maximum AXI interface performance.	–	333	MHz
$F_{DPLIVEVIDEO}$	DisplayPort controller live video interface maximum frequency.	–	300	MHz

PS I2C Controller Interface

Table 47: **I2C Interface**(1)

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µs
$T_{I2CSCKH}$	SCL High time.	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS-GTR Transceiver

Table 56: **PS-GTR Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.		75	–	$V_{PS\_MGTRAVCC}$	mV
V_{CMIN}	Common mode input voltage.		–	0	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.(1)	Transmitter output swing is set to maximum value.	800	–	–	mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{PS\_MGTRAVCC} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
$R_{MGTRREF}$	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–	20	ps
C_{EXT}	Recommended external AC coupling capacitor.(2)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: **PS-GTR Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 58: **PS-GTR Transceiver Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTRMAX}	PS-GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F_{GTRMIN}	PS-GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 59: **PS-GTR Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock.	–	–	0.11	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24×10^6	UI

Table 61: **PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$PLL_{REFCLKMASK}$	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

1. For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: **PS-GTR Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T_{RTX}	TX rise time.	20%–80%	–	65	–	ps
T_{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 63: **PS-GTR Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRRX}	Serial data rate.		1.25	–	6	Gb/s
RX_{SST}	Receiver spread-spectrum tracking.	Modulated at 33 KHz	–5000	–	0	ppm
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance.	All data rates	–350	–	350	ppm

Table 64: **PCI Express Protocol Characteristics (PS-GTR Transceivers)**(1)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter.	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter.	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance.	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error.	5000	0.4	–	UI
	Receiver inherent deterministic timing error.	5000	0.3	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 65: **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial ATA Transmitter Jitter Generation					
SATA Gen 1	Total transmitter jitter.	1500	–	0.37	UI
SATA Gen 2	Total transmitter jitter.	3000	–	0.37	UI
SATA Gen 3	Total transmitter jitter.	6000	–	0.52	UI
Serial ATA Receiver High Frequency Jitter Tolerance					
SATA Gen 1	Total receiver jitter tolerance.	1500	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	3000	0.27	–	UI
SATA Gen 2	Total receiver jitter tolerance.	6000	0.16	–	UI

Table 66: **DisplayPort Protocol Characteristics (PS-GTR Transceivers)**(1)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
DisplayPort Transmitter Jitter Generation					
RBR	Total transmitter jitter.	1620	–	0.42	UI
HBR	Total transmitter jitter.	2700	–	0.42	UI
HBR2 D10.2	Total transmitter jitter.	5400	–	0.40	UI
HBR2 CPAT	Total transmitter jitter.	5400	–	0.58	UI

Notes:

1. Only the transmitter is supported.

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 22. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3(3)		-2(3)		-1		-2(3)		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(4)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(4)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is $PLL\_F_{VCOMIN}/2$.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces *(Cont'd)***

Memory Standard	Package(1)	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
QDR II+	All	Single rank component(7)	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

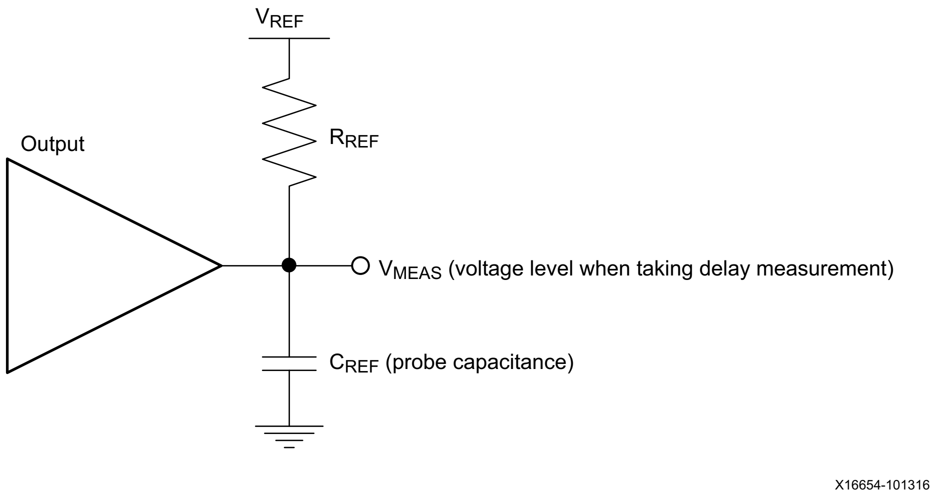

Figure 1: **Single-Ended Test Setup**

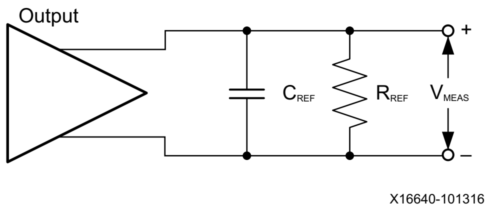

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 79.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

PLL Switching Characteristics

Table 86: **PLL Specification**[(1)]

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F$_{INMAX}$	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F$_{INMIN}$	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_F$_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F$_{INDUTY}$	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F$_{VCOMIN}$	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F$_{VCOMAX}$	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_T$_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
PLL_T$_{OUTJITTER}$	PLL output jitter.	Note 3					
PLL_T$_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
PLL_T$_{LOCKMAX}$	PLL maximum lock time.	100					µs
PLL_F$_{OUTMAX}$	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F$_{OUTMIN}$	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_RST$_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F$_{PFDMAX}$	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F$_{PFDMIN}$	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_F$_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	14	MHz
PLL_F$_{DPRCLK\_MAX}$	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]									
T_{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU2}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU3}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU4}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU5}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU6}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T_{PHFD_ZU7}		Hold		–0.40	–0.40	–0.40	–0.21	–0.21	ns
T_{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU9}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU11}		Hold		–0.29	–0.29	–0.29	–0.09	0.19	ns
T_{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T_{PHFD_ZU15}		Hold		–0.04	–0.04	–0.04	0.27	0.43	ns
T_{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU17}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns
T_{PSFD_ZU19}		Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU19}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 92: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T_{SAMP_BUFG} (1)	510	610	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	150	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	110	ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

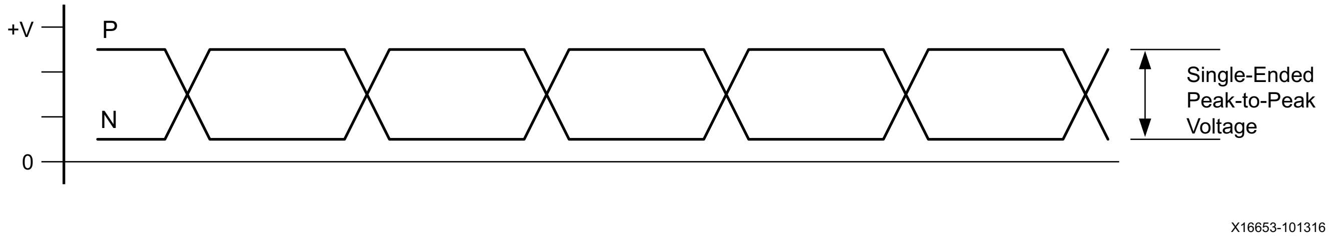

Figure 5: **Single-Ended Peak-to-Peak Voltage**

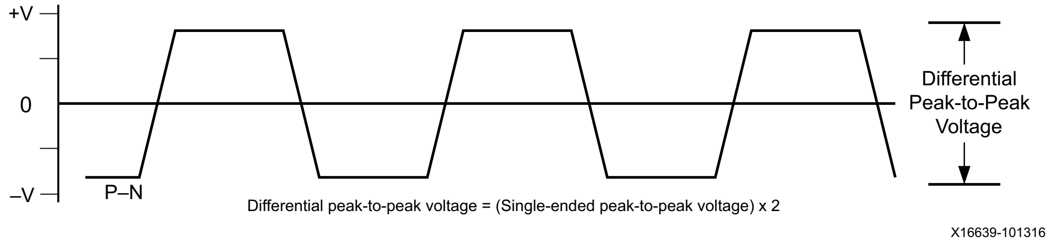

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

Table 114: **GTY Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).

Table 116: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Configuration Switching Characteristics

Table 127: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T_{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T_{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
$T_{PS\_PROG\_B}$	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max