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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 926K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu17eg-l2ffvc1760e

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
Video Codec Unit				
V_{CCINT_VCU}	Internal supply voltage for the video codec unit.	–0.500	1.000	V
PL System Monitor				
V_{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature.(12)	–	260	°C
T_j	Maximum junction temperature.(12)	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
7. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
12. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{CCO}(8)	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(9)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(10)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(11)	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$(12)	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(12)	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$(12)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$(12)	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V_{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks(1)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 19: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks(1)**

I/O Standard	V_{ICM} (V)(2)			V_{ID} (V)(3)		V_{OL} (V)(4)	V_{OH} (V)(5)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	($V_{CCO}/2$) – 0.120	$V_{CCO}/2$	($V_{CCO}/2$) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	8.0	–8.0
DIFF_SSTL135	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	9.0	–9.0
DIFF_SSTL15	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.175	($V_{CCO}/2$) + 0.175	10.0	–10.0
DIFF_SSTL18_I	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.470	($V_{CCO}/2$) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: **Table 21 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCZU2CG	N/A	Vivado tools 2017.1 v1.10					
XCZU2EG	N/A	Vivado tools 2017.1 v1.10					
XCZU3CG	N/A	Vivado tools 2017.1 v1.10					
XCZU3EG	N/A	Vivado tools 2017.1 v1.10					
XCZU4CG	N/A						
XCZU4EG							
XCZU4EV							
XCZU5CG	N/A						
XCZU5EG							
XCZU5EV							
XCZU6CG	N/A	Vivado tools 2017.1 v1.10					
XCZU6EG		Vivado tools 2017.1 v1.10					
XCZU7CG	N/A						
XCZU7EG							
XCZU7EV							
XCZU9CG	N/A	Vivado tools 2017.1 v1.10					
XCZU9EG		Vivado tools 2017.1 v1.10					
XCZU11EG							
XCZU15EG							
XCZU17EG							
XCZU19EG							

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Table 67: **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –55°C to 110°C	–	–	±3.5	°C
		T_j = 110°C to 125°C	–	–	±5	°C
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	T_j = –40°C to 125°C	–	–	±2.5	%

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 77: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

Table 78: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

PLL Switching Characteristics

Table 86: **PLL Specification(1)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3					
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100					µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T_{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU2}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU3}		Hold			–0.36	–0.36	–0.14	–0.14	ns
T_{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU4}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU5}		Hold		–0.28	–0.28	–0.28	–0.09	–0.09	ns
T_{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU6}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T_{PHFD_ZU7}		Hold		–0.40	–0.40	–0.40	–0.21	–0.21	ns
T_{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU9}		Hold		–0.05	–0.05	–0.05	0.27	0.42	ns
T_{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU11}		Hold		–0.29	–0.29	–0.29	–0.09	0.19	ns
T_{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T_{PHFD_ZU15}		Hold		–0.04	–0.04	–0.04	0.27	0.43	ns
T_{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU17}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns
T_{PSFD_ZU19}		Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU19}		Hold		–0.38	–0.38	–0.38	–0.19	–0.19	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 93: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCZU2	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU3	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU4	SFVC784		ps
			FBVB900		ps
		XCZU5	SFVC784		ps
			FBVB900		ps
		XCZU6	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU7	FBVB900	141	ps
			FFVC1156	175	ps
			FFVF1517	305	ps
		XCZU9	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU11	FFVC1156		ps
			FFVB1517		ps
			FFVF1517		ps
			FFVC1760	215	ps
		XCZU15	FFVC900	118	ps
			FFVB1156	132	ps
		XCZU17	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps
		XCZU19	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 106 and Table 107 summarize the DC specifications of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 106: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

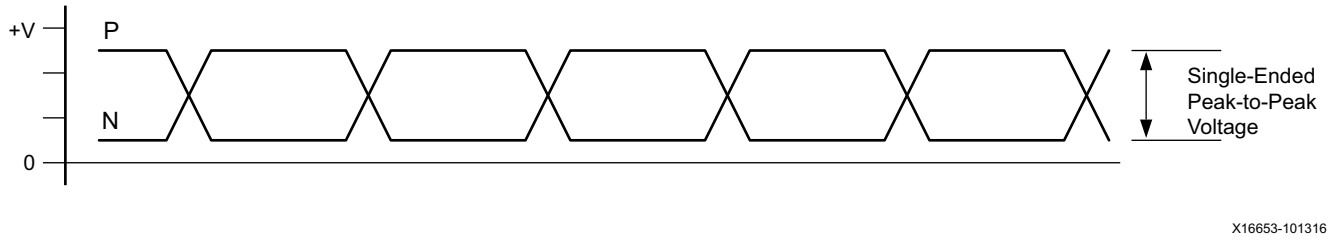

Figure 5: **Single-Ended Peak-to-Peak Voltage**

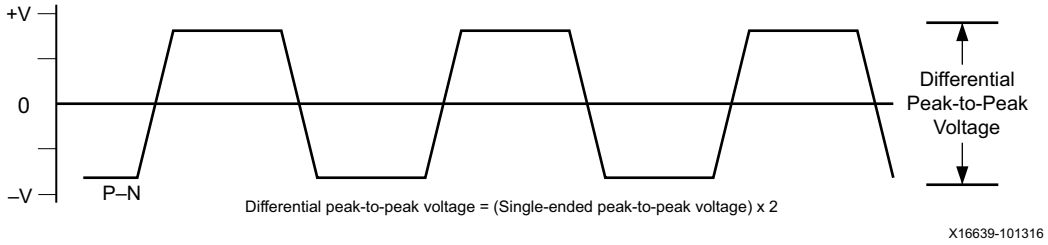

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 109: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range(1)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range(2)	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range(3)	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 116: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 117: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Video Codec Performance

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 123: **VCU Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 124: **PL SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity(2)	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic (T_j = –55°C to 125°C)	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: –2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: –2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: –2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: –2E, -2I, -1E, -1I Added -2E (V_{CCINT} = 0.85V) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{RFPSCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the *PS NAND Memory Controller Interface* section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU\_REF\_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the PS-GTR Transceiver section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90,and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPPOUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPPOUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the Integrated Interface Block for Interlaken and Integrated Interface Block for 100G Ethernet MAC and PCS sections. Revised the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3.