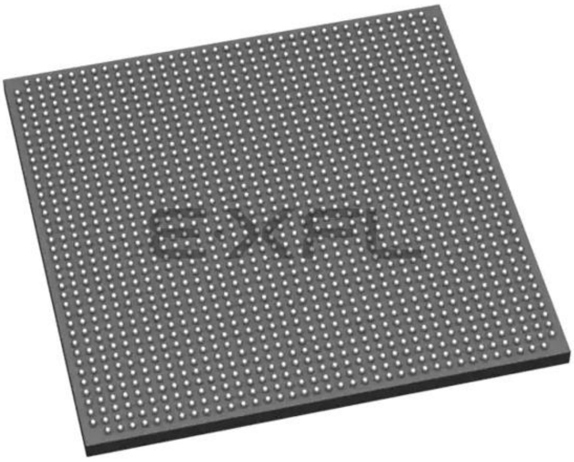
AMD Xilinx - XCZU19EG-2FFVB1517I Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 1143K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu19eg-2ffvb1517i

Table 8: **V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks[(1)]**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO_PSIO} + 0.30	100%	–0.30	100%
V_{CCO_PSIO} + 0.35	100%	–0.35	75%
V_{CCO_PSIO} + 0.40	100%	–0.40	45%
V_{CCO_PSIO} + 0.45	100%	–0.45	40%
V_{CCO_PSIO} + 0.50	75%	–0.50	10%
V_{CCO_PSIO} + 0.55	75%	–0.55	6%
V_{CCO_PSIO} + 0.60	60%	–0.60	2%
V_{CCO_PSIO} + 0.65	30%	–0.65	0%
V_{CCO_PSIO} + 0.70	20%	–0.70	0%
V_{CCO_PSIO} + 0.75	10%	–0.75	0%
V_{CCO_PSIO} + 0.80	10%	–0.80	0%
V_{CCO_PSIO} + 0.85	8%	–0.85	0%
V_{CCO_PSIO} + 0.90	6%	–0.90	0%
V_{CCO_PSIO} + 0.95	6%	–0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTLP}$
2. V_{CC_PSAUX}, V_{CC_PSADC}, and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTFP}$ and $V_{CC\_PSINTFP\_DDR}$ driven from the same supply source.
2. $V_{PS\_MGTRAVCC}$ and $V_{CC\_PSDDR\_PLL}$ in any order or simultaneously.
3. $V_{PS\_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 10: **Power-on Current by Device**[(1)]

I_{CC} Min =	I_{CCQ} +	XCZU2	XCZU3	XCZU4	XCZU5	XCZU6	XCZU7	XCZU9	XCZU11	XCZU15	XCZU17	XCZU19	Units
$I_{CCINTMIN}$	I_{CCINTQ} +	464	464	770	770	1800	1514	1800	1961	2242	3433	3433	mA
I_{CCINT_IOMIN} + $I_{CCBRAMMIN}$	$I_{CCBRAMQ}$ + I_{CCINT_IOQ} +	155	155	257	257	600	505	600	654	748	1145	1145	mA
I_{CCOMIN}	I_{CCOQ} +	50	50	50	50	50	50	50	55	63	96	96	mA
$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	I_{CCAUXQ} + I_{CCAUX_IOQ} +	111	111	386	386	650	362	650	709	810	1240	1240	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

Table 11: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}.	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}.	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU}.	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}.	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}.	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}.	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms
$T_{VCC\_PSINTFP}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP}$.	0.2	40	ms
$T_{VCC\_PSINTLP}$	Ramp time from GND to 95% of $V_{CC\_PSINTLP}$.	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX}.	0.2	40	ms
$T_{VCC\_PSINTFP\_DDR}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP\_DDR}$.	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC}.	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL}.	0.2	40	ms
$T_{PS\_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVCC}$.	0.2	40	ms
$T_{PS\_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVTT}$.	0.2	40	ms

Table 17: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)[1]			V_{ID}(V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM}(V)[4]			V_{OD}(V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS[8]	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS[9]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage ($Q - \overline{Q}$).
6. LVDS_25 is specified in Table 23.
7. LVDS is specified in Table 24.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU11EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU17EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

PS Configuration

Table 39: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: **Boundary-Scan Port Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS I2C Controller Interface

Table 47: **I2C Interface**[1]

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µs
$T_{I2CSCKH}$	SCL High time.	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SPI Controller Interface

Table 48: **SPI Interfaces[1]**

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge.	1[2]	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1[2]	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: **CAN Interface[1]**

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Triple-timer Counter Interface

Table 54: **Triple-timer Counter Interface**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	–	16.5	MHz
$T_{TTCICLKL}$	Triple-timer counter input clock high pulse width.	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$T_{TTCICLKH}$	Triple-timer counter input clock low pulse width.	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	–	$F_{LPD\_LSBUS\_CTRLMAX}$/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: **Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

Table 67: **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –55°C to 110°C	–	–	±3.5	°C
		T_j = 110°C to 125°C	–	–	±5	°C
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	T_j = –40°C to 125°C	–	–	±2.5	%

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_F	0.856	0.856	0.900	0.856	0.900	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
HSTL_I_S	0.856	0.856	0.900	0.856	0.900	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
HSUL_12_F	0.780	0.780	0.867	0.780	0.867	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
HSUL_12_S	0.780	0.780	0.867	0.780	0.867	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
LVCMOS12_F_12	0.918	0.918	0.976	0.918	0.976	1.689	1.689	1.856	1.689	1.856	1.202	1.202	1.317	1.202	1.317	ns
LVCMOS12_F_4	0.918	0.918	0.976	0.918	0.976	1.742	1.742	1.922	1.742	1.922	1.353	1.353	1.478	1.353	1.478	ns
LVCMOS12_F_8	0.918	0.918	0.976	0.918	0.976	1.714	1.714	1.879	1.714	1.879	1.292	1.292	1.432	1.292	1.432	ns
LVCMOS12_S_12	0.918	0.918	0.976	0.918	0.976	2.073	2.073	2.247	2.073	2.247	1.581	1.581	1.717	1.581	1.717	ns
LVCMOS12_S_4	0.918	0.918	0.976	0.918	0.976	1.979	1.979	2.182	1.979	2.182	1.633	1.633	1.772	1.633	1.772	ns
LVCMOS12_S_8	0.918	0.918	0.976	0.918	0.976	2.205	2.205	2.406	2.205	2.406	1.767	1.767	1.928	1.767	1.928	ns
LVCMOS15_F_12	0.905	0.905	0.958	0.905	0.958	1.713	1.713	1.892	1.713	1.892	1.275	1.275	1.428	1.275	1.428	ns
LVCMOS15_F_16	0.905	0.905	0.958	0.905	0.958	1.722	1.722	1.881	1.722	1.881	1.260	1.260	1.407	1.260	1.407	ns
LVCMOS15_F_4	0.905	0.905	0.958	0.905	0.958	1.825	1.825	1.959	1.825	1.959	1.453	1.453	1.557	1.453	1.557	ns
LVCMOS15_F_8	0.905	0.905	0.958	0.905	0.958	1.778	1.778	1.930	1.778	1.930	1.378	1.378	1.458	1.378	1.458	ns
LVCMOS15_S_12	0.905	0.905	0.958	0.905	0.958	1.991	1.991	2.139	1.991	2.139	1.516	1.516	1.648	1.516	1.648	ns
LVCMOS15_S_16	0.905	0.905	0.958	0.905	0.958	2.172	2.172	2.389	2.172	2.389	1.707	1.707	1.888	1.707	1.888	ns
LVCMOS15_S_4	0.905	0.905	0.958	0.905	0.958	2.313	2.313	2.483	2.313	2.483	1.952	1.952	2.123	1.952	2.123	ns
LVCMOS15_S_8	0.905	0.905	0.958	0.905	0.958	2.170	2.170	2.400	2.170	2.400	1.817	1.817	1.984	1.817	1.984	ns
LVCMOS18_F_12	0.915	0.915	0.958	0.915	0.958	1.805	1.805	1.962	1.805	1.962	1.383	1.383	1.471	1.383	1.471	ns
LVCMOS18_F_16	0.915	0.915	0.958	0.915	0.958	1.785	1.785	1.917	1.785	1.917	1.338	1.338	1.446	1.338	1.446	ns
LVCMOS18_F_4	0.915	0.915	0.958	0.915	0.958	1.868	1.868	2.013	1.868	2.013	1.472	1.472	1.599	1.472	1.599	ns
LVCMOS18_F_8	0.915	0.915	0.958	0.915	0.958	1.797	1.797	1.979	1.797	1.979	1.384	1.384	1.487	1.384	1.487	ns
LVCMOS18_S_12	0.915	0.915	0.958	0.915	0.958	2.201	2.201	2.408	2.201	2.408	1.762	1.762	1.894	1.762	1.894	ns
LVCMOS18_S_16	0.915	0.915	0.958	0.915	0.958	2.173	2.173	2.362	2.173	2.362	1.702	1.702	1.834	1.702	1.834	ns
LVCMOS18_S_4	0.915	0.915	0.958	0.915	0.958	2.346	2.346	2.567	2.346	2.567	1.951	1.951	2.092	1.951	2.092	ns
LVCMOS18_S_8	0.915	0.915	0.958	0.915	0.958	2.292	2.292	2.511	2.292	2.511	1.848	1.848	2.008	1.848	2.008	ns
LVCMOS25_F_12	0.988	0.988	1.042	0.988	1.042	2.153	2.153	2.453	2.153	2.453	1.692	1.692	1.856	1.692	1.856	ns
LVCMOS25_F_16	0.988	0.988	1.042	0.988	1.042	2.105	2.105	2.406	2.105	2.406	1.623	1.623	1.786	1.623	1.786	ns
LVCMOS25_F_4	0.988	0.988	1.042	0.988	1.042	2.344	2.344	2.554	2.344	2.554	1.842	1.842	2.039	1.842	2.039	ns
LVCMOS25_F_8	0.988	0.988	1.042	0.988	1.042	2.184	2.184	2.516	2.184	2.516	1.726	1.726	1.910	1.726	1.910	ns
LVCMOS25_S_12	0.988	0.988	1.042	0.988	1.042	2.558	2.558	2.840	2.558	2.840	1.971	1.971	2.194	1.971	2.194	ns
LVCMOS25_S_16	0.988	0.988	1.042	0.988	1.042	2.449	2.449	2.740	2.449	2.740	1.852	1.852	2.063	1.852	2.063	ns
LVCMOS25_S_4	0.988	0.988	1.042	0.988	1.042	2.770	2.770	3.066	2.770	3.066	2.224	2.224	2.458	2.224	2.458	ns
LVCMOS25_S_8	0.988	0.988	1.042	0.988	1.042	2.663	2.663	2.963	2.663	2.963	2.091	2.091	2.373	2.091	2.373	ns
LVCMOS33_F_12	1.154	1.154	1.213	1.154	1.213	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVCMOS33_F_16	1.154	1.154	1.213	1.154	1.213	2.383	2.383	2.603	2.383	2.603	1.734	1.734	1.869	1.734	1.869	ns
LVCMOS33_F_4	1.154	1.154	1.213	1.154	1.213	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVCMOS33_F_8	1.154	1.154	1.213	1.154	1.213	2.603	2.603	2.822	2.603	2.822	1.937	1.937	2.130	1.937	2.130	ns
LVCMOS33_S_12	1.154	1.154	1.213	1.154	1.213	2.705	2.705	3.047	2.705	3.047	2.049	2.049	2.318	2.049	2.318	ns
LVCMOS33_S_16	1.154	1.154	1.213	1.154	1.213	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVCMOS33_S_4	1.154	1.154	1.213	1.154	1.213	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Table 78: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} [1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Table 99: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 100: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$(1)(2)	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$(1)(2)	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:
1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 101: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 102: **GTH Transceiver User Clock Switching Characteristics**(1)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)(5)	-2(3)	-1(5)	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 118).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 119).
- 12 x 25.78125 Gb/s lane logic only mode (Table 120).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 109 for the F_{GTYMAX} description.

Table 118: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 124: **PL SYSMON Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error(1)(3)		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C
Supply sensor error(4)		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate(5)						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference(6)						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.