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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 1143K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu19eg-2ffvc1760i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
V _{CCO_PSDDR}	PS DDR I/O supply voltage.	−0.500	1.650	V
V _{CC_PSDDR_PLL}	PS DDR PLL supply voltage.	−0.500	2.000	V
V _{CCO_PSIO}	PS I/O supply.	−0.500	3.630	V
V _{PSIN} ⁽²⁾	PS I/O input voltage.	−0.500	V _{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	−0.500	V _{CCO_PSDDR} + 0.550	V
V _{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	−0.500	2.000	V
Programmable Logic (PL)				
V _{CCINT}	Internal supply voltage.	−0.500	1.000	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks.	−0.500	1.000	V
V _{CCAUX}	Auxiliary supply voltage.	−0.500	2.000	V
V _{CCBRAM}	Supply voltage for the block RAM memories.	−0.500	1.000	V
V _{CCO}	Output drivers supply voltage for HD I/O banks.	−0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	−0.500	2.000	V
V _{CCAUX_IO} ⁽⁴⁾	Auxiliary supply voltage for the I/O banks.	−0.500	2.000	V
V _{REF}	Input reference voltage.	−0.500	2.000	V
V _{IN} ⁽²⁾⁽⁵⁾⁽⁷⁾	I/O input voltage for HD I/O banks. ⁽⁶⁾	−0.550	V _{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	−0.550	V _{CCO} + 0.550	V
I _{DC}	Available output current at the pad.	−20	20	mA
I _{RMS}	Available RMS output current at the pad.	−20	20	mA
GTH or GTY Transceiver				
V _{MGTAVCC}	Analog supply voltage for transceiver circuits.	−0.500	1.000	V
V _{MGTAVTT}	Analog supply voltage for transceiver termination circuits.	−0.500	1.300	V
V _{MGTVCCAUX}	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	−0.500	1.900	V
V _{MGTREFCLK}	Transceiver reference clock absolute input voltage.	−0.500	1.300	V
V _{MGTAVTTRCAL}	Analog supply voltage for the resistor calibration circuit of the transceiver column.	−0.500	1.300	V
V _{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	−0.500	1.200	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating. ⁽⁸⁾	—	10	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT} .	—	10	mA
I _{DCIN-GND}	DC input current for receiver input pins DC coupled RX termination = GND. ⁽⁹⁾	—	0	mA
I _{DCIN-PROG}	DC input current for receiver input pins DC coupled RX termination = programmable. ⁽¹⁰⁾	—	0	mA
I _{DCOUT-FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating.	—	6	mA
I _{DCOUT-MGTAVTT}	DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} .	—	6	mA

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTAVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V_{ICM} (V) ⁽²⁾			V_{ID} (V) ⁽³⁾		V_{OL} (V) ⁽⁴⁾	V_{OH} (V) ⁽⁵⁾	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: Table 21 Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 23: LVDS_25 DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	100	350	600 ⁽²⁾	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 24: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		1.710	1.800	1.890	V
$V_{ODIFF}^{(2)}$	Differential output voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
$V_{OCM}^{(2)}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
$V_{IDIFF}^{(3)}$	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$		100	350	600 ⁽³⁾	mV
$V_{ICM_DC}^{(4)}$	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
$V_{ICM_AC}^{(5)}$	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release

Device	Speed Grade and V _{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCZU2CG	N/A	Vivado tools 2017.1 v1.10					
XCZU2EG	N/A	Vivado tools 2017.1 v1.10					
XCZU3CG	N/A	Vivado tools 2017.1 v1.10					
XCZU3EG	N/A	Vivado tools 2017.1 v1.10					
XCZU4CG	N/A						
XCZU4EG							
XCZU4EV							
XCZU5CG	N/A						
XCZU5EG							
XCZU5EV							
XCZU6CG	N/A	Vivado tools 2017.1 v1.10					
XCZU6EG		Vivado tools 2017.1 v1.10					
XCZU7CG	N/A						
XCZU7EG							
XCZU7EV							
XCZU9CG	N/A	Vivado tools 2017.1 v1.10					
XCZU9EG		Vivado tools 2017.1 v1.10					
XCZU11EG							
XCZU15EG							
XCZU17EG							
XCZU19EG							

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: Generic Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK1}	Quad-SPI clock duty cycle.	15 pF	45	55	%
T _{QSPISSSCLK1}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
T _{QSPISCLKSS1}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
T _{QSPICKO1}	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
T _{QSPIDCK1}	Setup time, all inputs.	15 pF	0.9	–	ns
T _{QSPICKD1}	Hold time, all inputs.	15 pF	1.0	–	ns
F _{QSPICLK1}	Quad-SPI device clock frequency.	15 pF	–	150	MHz
F _{QSPIREFCLK1}	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK2}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSSCLK2}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS2}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO2}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK2}	Setup time, all inputs.	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
T _{QSPICKD2}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPICLK2}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
F _{QSPIREFCLK2}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz

Notes:

- The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
- 30 pF loads are for dual-parallel stacked or stacked modes.

Table 42: Linear Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK5}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSCLK5}	Slave select asserted to next clock edge. ⁽³⁾	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS5}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO5}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK5}	Setup time, all inputs.	15 pF	2.4	–	ns
		30 pF	2.4	–	ns
T _{QSPICKD5}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPIREFCLK5}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
F _{QSPICLK5}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. T_{QSPISSCLK5} is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: ULPI Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T _{ULPIDCK}	Input setup to ULPI clock, all inputs.	4.5	–	ns
T _{ULPICKD}	Input hold to ULPI clock, all inputs.	0	–	ns
T _{ULPICKO}	ULPI clock to output valid, all outputs.	2.0	8.86	ns
F _{ULPICLK}	ULPI reference clock frequency.	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Gigabit Ethernet Controller Interface

Table 44: RGMII Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T _{DCGEMTXCLK}	Transmit clock duty cycle.	45	55	%
T _{GEMTXCKO}	TXD output clock to out time.	–0.5	0.5	ns
T _{GEMRXDCK}	RXD input setup time.	0.8	–	ns
T _{GEMRXCKD}	RXD input hold time.	0.8	–	ns
T _{MDIOCLK}	MDC output clock period.	400	–	ns
T _{MDIOCKL}	MDC low time.	160	–	ns
T _{MDIOCKH}	MDC high time.	160	–	ns
T _{MDIODCK}	MDIO input data setup time.	80	–	ns
T _{MDIOCKD}	MDIO input data hold time.	0.0	–	ns
T _{MDIOCKO}	MDIO output data delay time.	–1.0	15	ns
F _{GETXCLK}	RGMII_TX_CLK transmit clock frequency.	–	125	MHz
F _{GERXCLK}	RGMII_RX_CLK receive clock frequency.	–	125	MHz
F _{ENET_REF_CLK}	Ethernet reference clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SD/SDIO Controller Interface

Table 45: SD/SDIO Interface⁽¹⁾

Symbol	Description	Min	Max	Units
SD/SDIO Interface DDR50 Mode				
T _{DCDDRCLK}	SD device clock duty cycle.	45	55	%
T _{SDDDRCKO1}	Clock to output delay, data. ⁽²⁾	1.0	6.8	ns
T _{SDDRIVW}	Input valid data window. ⁽³⁾	3.5	–	ns
T _{SDDDRDCK2}	Input setup time, command.	4.7	–	ns
T _{SDDDRCKD2}	Input hold time, command.	1.5	–	ns
T _{SDDDRCKO2}	Clock to output delay, command.	1.0	13.8	ns
F _{SDDDRCLK}	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface SDR104				
T _{DCSDHCLK1}	SD device clock duty cycle.	40	60	%
T _{SDSDRCKO1}	Clock to output delay, all outputs. ⁽²⁾	1.0	3.2	ns
T _{SSDSR1IVW}	Input valid data window. ⁽³⁾	0.5	–	UI
F _{SDSDRCLK1}	SDR104 mode device clock frequency.	–	200	MHz
SD/SDIO Interface SDR50/25				
T _{DCSDHCLK2}	SD device clock duty cycle.	40	60	%
T _{SDSDRCKO2}	Clock to output delay, all outputs. ⁽²⁾	1.0	6.8	ns
T _{SSDSR2IVW}	Input valid data window. ⁽³⁾	0.3	–	UI

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3 (1)	-2 (1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces (Cont'd)

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	800	800	800	800	606	Mb/s
QDR II +	All	Single rank component ⁽⁷⁾	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF_DELAY_PAD_I}}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF_DELAY_O_PAD}}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF_DELAY_TD_PAD}}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{\text{OUTBUF_DELAY_TD_PAD}}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I / O Standards	$T_{\text{INBUF_DELAY_PAD_I}}$					$T_{\text{OUTBUF_DELAY_O_PAD}}$					$T_{\text{OUTBUF_DELAY_TD_PAD}}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVC MOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVC MOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVC MOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVC MOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVC MOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVC MOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVC MOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVC MOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVC MOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVC MOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVC MOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVC MOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVC MOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVC MOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVC MOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVC MOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVC MOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVC MOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVC MOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVC MOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVC MOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVC MOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVC MOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVC MOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVC MOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVC MOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVC MOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVC MOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVC MOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVC MOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVC MOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Device Pin-to-Pin Output Parameter Guidelines

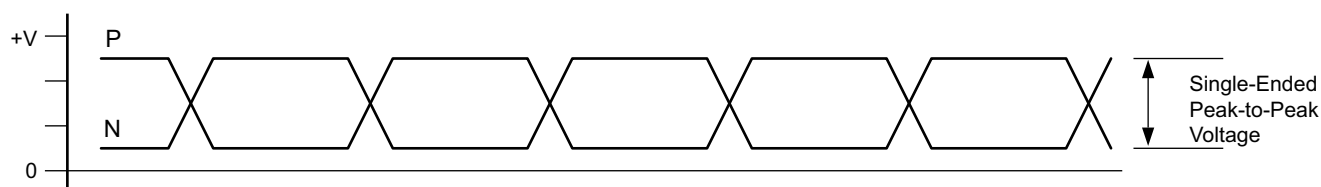
The pin-to-pin numbers in [Table 87](#) through [Table 89](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 87: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.								
T _{ICKOF}	Global clock input and output flip-flop <i>without</i> MMCM (near clock region).	XCZU2	N/A	4.90	5.28	5.35	5.61	ns
		XCZU3	N/A	4.90	5.28	5.35	5.61	ns
		XCZU4	4.89	5.83	6.36	6.00	6.79	ns
		XCZU5	4.89	5.83	6.36	6.00	6.79	ns
		XCZU6	5.00	5.91	6.35	6.66	7.09	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.00	5.91	6.35	6.66	7.09	ns
		XCZU11	5.82	6.96	7.61	7.19	8.36	ns
		XCZU15	5.15	6.09	6.55	6.90	7.38	ns
		XCZU17	5.72	6.90	7.40	7.62	8.07	ns
XCZU19	5.72	6.90	7.40	7.62	8.07	ns		

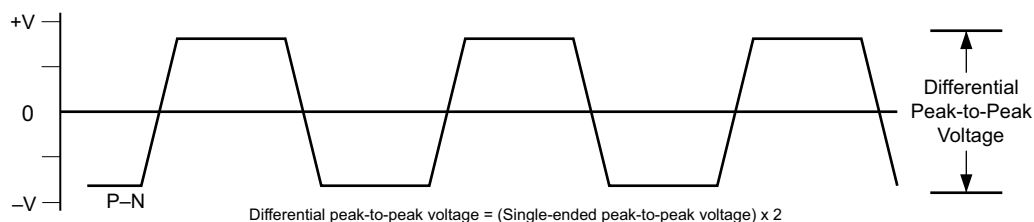
Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.



X16653-101316

Figure 3: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 4: Differential Peak-to-Peak Voltage

Table 95 and Table 96 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 95: GTH Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 96: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N.	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N.	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage. (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage.	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 109: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F _{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYCRANGE}	CPLL line rate range ⁽¹⁾	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE1}	QPLL0 line rate range ⁽²⁾	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE2}	QPLL1 line rate range ⁽³⁾	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL0_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 114: GTY Transceiver User Clock Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXIN2}	TXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz
F _{RXIN2}	RXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz

Notes:

- Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).

Table 115: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: -2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: -2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: -2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: -2E, -2I, -1E, -1I Added -2E ($V_{CCINT} = 0.85V$) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{REFPCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the <i>PS NAND Memory Controller Interface</i> section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU_REF_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the <i>PS-GTR Transceiver</i> section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90, and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPPOUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPPOUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the <i>Integrated Interface Block for Interlaken</i> and <i>Integrated Interface Block for 100G Ethernet MAC and PCS</i> sections. Revised the <i>Configuration Switching Characteristics</i> section. Removed the <i>eFUSE Programming Conditions</i> table and added the specifications to Table 2 and Table 3.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1 . Updated Table 2 , Table 4 , Table 6 , Table 7 , and Table 9 . Revised the Power Supply Sequencing section including Table 10 . Added PS and VCU ramp times to Table 11 . Revised V_{ODIFF} in Table 24 . Updated Table 25 . Added Note 1 to Table 26 . Table 30 replaces the previous three PS memory performance tables. Added values to Table 34 , Table 37 , and Table 38 . Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40 . Added Note 3 to Table 41 . Added Note 3 to Table 42 . Added Note 1 to Table 45 . Updated Table 48 and removed Note 3 . Added data to Table 56 . Updated Table 60 . Added Table 61 . Updated Table 63 . Revised Table 69 . Added data to Table 70 . Added Note 2 to Table 71 . Updated Table 74 and added Note 4 . Updated V_L and V_H values in Table 78 . Added T_{MINPER_CLK} , revised F_{REFCLK} , and Note 1 to Table 82 . Added $MMCM_F_{DPRCLK_MAX}$ to Table 85 and $PLL_F_{DPRCLK_MAX}$ to Table 86 . Added data to Table 94 , Table 96 , Table 98 , Table 101 , and updated the note references in Table 102 . Updated Table 103 and added Note 8 . Updated Table 104 and added Note 7 . Added more protocols, Note 1 and Note 2 to Table 105 . Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 105 . Added Note 1 to Table 109 . Added data to Table 106 , Table 108 , Table 110 , Table 113 . Added Note 2 to Table 112 . Added note references in Table 114 . Updated Table 115 and added Note 8 . Updated Table 116 and added Note 7 . Added more protocols and Note 3 to Table 117 . Removed the GTy Transceiver Protocol Jitter Characteristics section because it is covered in Table 117 . Revised Table 124 . Added T_{POR} and updated F_{ICAPCK} in Table 127 . Updated the Automotive Applications Disclaimer .
06/20/2016	1.1	Updated the Summary description. In Table 1 , revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU} , I_{RPD} , and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5 . Updated Note 5 in Table 4 . Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added $MIPI_DPHY_DCI$ to Table 14 , Table 15 , and Table 17 . Updated Table 23 , including removing the V_{CCO} specification and adding Note 1 . Added Note 1 to Table 24 . Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28 . Updated the -2 value in Table 29 . Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33 . Added VCO frequencies to Table 36 . Added the T_{PSPOR} minimum to Table 37 and updated Note 1 . Added Table 38 . Added value delineation over V_{CCINT} operating voltages in Table 39 . Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42 . Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43 . Added $F_{TSI_REF_CLK}$ to Table 44 and updated Note 1 . In Table 45 , revised $T_{DCSDHCLK1}$, $T_{DCSDHCLK2}$, and $T_{DCSDHCLK3}$ and Note 1 . In Table 46 , revised Note 1 . In Table 47 , revised Note 1 . Revised Table 48 , including Note 1 , and added Note 2 and Note 3 . In Table 49 , Table 50 , Table 51 , and Table 53 , revised Note 1 . Updated Table 71 . Replaced Table 74 . Updated Table 75 and Table 76 . Updated Table 78 and Table 79 . In Table 80 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95 . Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97 . Added Table 100 and Table 112 . Added Note 2 to Table 106 . Revised data in Table 109 . Revised Table 114 . Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121 . Moved Table 123 . Revised INL in Table 124 . Added notes to Table 125 and Table 126 . In the eFUSE and Programming Conditions table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.