AMD Xilinx - XCZU19EG-2FFVD1760I Datasheet

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 600MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 1143K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu19eg-2ffvd1760i

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions**(1)(2)

Symbol	Description	Min	Typ	Max	Units
Processor System					
$V_{CC\_PSINTFP}$[3]	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
$V_{CC\_PSINTFP\_DDR}$[3]	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage.	0.825	0.850	0.875	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage.	1.746	1.800	1.854	V
V_{CCO_PSDDR}[4]	PS DDR I/O supply voltage.	1.06	–	1.575	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V_{CCO_PSIO}[5]	PS I/O supply.	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage.	–0.200	–	V_{CCO_PSIO} + 0.200	V
	PS DDR I/O input voltage.	–0.200	–	V_{CCO_PSDDR} + 0.200	
V_{CC_PSBATT}[6]	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	1.200	–	1.500	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}[7]	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V

Table 2: **Recommended Operating Conditions**[1][2] ***(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{CCO}[8]	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}[9]	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}[10]	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[11]	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$[12]	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$[12]	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$[12]	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$[12]	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V_{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
I_{CC_PSBATT}(4)(5)	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC enabled.	–	–	3650	nA
	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC disabled.	–	–	650	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC enabled.	–	–	3150	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC disabled.	–	–	150	nA
I_{PSFS}(6)	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in HP I/O banks(8) (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%(7)	40	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%(7)	48	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%(7)	60	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%(7)	120	+10%(7)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%(7)	240	+10%(7)	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V

Table 11: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**(1)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	–0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	–12
LVCMOS25	–0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	–12
LVCMOS18	–0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} – 0.45	12	–12

Notes:

1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**(1)

DDR Standard	V_{IL}		V_{IH}		V_{OL}(2)	V_{OH}(2)	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} – 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	–0.1
LPDDR4	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} – 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	–10
DDR3	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	–8
LPDDR3	0.000	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8
DDR3L	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} – 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	–8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU2EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU4CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Table 45: **SD/SDIO Interface(1)** ***(Cont'd)***

Symbol	Description	Min	Max	Units
$F_{SDSDRCLK2}$	SDR50 mode device clock frequency.	–	100	MHz
	SDR25 mode device clock frequency.	–	50	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs.	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs.	24.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle.	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs.(2)	2.2	13.8	ns
$T_{SDHSDIVW}$	Input valid data window.(3)	0.35	–	UI
$F_{SDHSCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle.	45	55	%
T_{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs.	2.0	–	ns
$F_{SDIDCLK}$	Clock frequency in identification mode.	–	400	KHz
F_{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS Triple-timer Counter Interface

Table 54: **Triple-timer Counter Interface**

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	–	16.5	MHz
$T_{TTCICLKL}$	Triple-timer counter input clock high pulse width.	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$T_{TTCICLKH}$	Triple-timer counter input clock low pulse width.	1.5 x 1/$F_{LPD\_LSBUS\_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	–	$F_{LPD\_LSBUS\_CTRLMAX}$/3	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: **Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

Table 61: **PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$PLL_{REFCLKMASK}$	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

1. For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: **PS-GTR Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T_{RTX}	TX rise time.	20%–80%	–	65	–	ps
T_{FTX}	TX fall time.	80%–20%	–	65	–	ps

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 22. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3(3)		-2(3)		-1		-2(3)		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(4)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(4)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is $PLL\_F_{VCOMIN}/2$.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 72: **MIPI D-PHY Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3(1)	-2(1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: **LVDS Native-Mode 1000BASE-X Support(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	Package(1)	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM(2)(3)(4)	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM(2)(5)	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM(2)(6)	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM(2)(3)	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM(2)(5)	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM(2)(3)	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM(2)(5)	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM(2)(6)	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM(2)(5)	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM(2)(6)	1066	1066	1066	1066	800	Mb/s

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	**0.85V**		**0.72V**		**0.90V**	**0.85V**		**0.72V**		**0.90V**	**0.85V**		**0.72V**		
	-3	**-2**	**-1**	**-2**	**-1**	**-3**	**-2**	**-1**	**-2**	**-1**	**-3**	**-2**	**-1**	**-2**	**-1**	
LVCMOS33_S_8	1.154	1.154	1.213	1.154	1.213	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
LVDS_25	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.164	1.223	1.164	1.223	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVTTL_F_16	1.164	1.164	1.223	1.164	1.223	2.464	2.464	2.732	2.464	2.732	1.750	1.750	1.986	1.750	1.986	ns
LVTTL_F_4	1.164	1.164	1.223	1.164	1.223	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVTTL_F_8	1.164	1.164	1.223	1.164	1.223	2.582	2.582	2.787	2.582	2.787	1.910	1.910	2.063	1.910	2.063	ns
LVTTL_S_12	1.164	1.164	1.223	1.164	1.223	2.731	2.731	3.075	2.731	3.075	2.072	2.072	2.343	2.072	2.343	ns
LVTTL_S_16	1.164	1.164	1.223	1.164	1.223	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVTTL_S_4	1.164	1.164	1.223	1.164	1.223	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns
LVTTL_S_8	1.164	1.164	1.223	1.164	1.223	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
SLVS_400_25	1.020	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.780	0.867	0.780	0.867	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
SSTL12_S	0.780	0.780	0.867	0.780	0.867	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
SSTL135_F	0.798	0.798	0.881	0.798	0.881	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
SSTL135_II_F	0.798	0.798	0.881	0.798	0.881	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
SSTL135_II_S	0.798	0.798	0.881	0.798	0.881	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
SSTL135_S	0.798	0.798	0.881	0.798	0.881	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
SSTL15_F	0.838	0.838	0.880	0.838	0.880	1.612	1.612	1.754	1.612	1.754	1.357	1.357	1.464	1.357	1.464	ns
SSTL15_II_F	0.838	0.838	0.880	0.838	0.880	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
SSTL15_II_S	0.838	0.838	0.880	0.838	0.880	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
SSTL15_S	0.838	0.838	0.880	0.838	0.880	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
SSTL18_II_F	0.947	0.947	1.021	0.947	1.021	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
SSTL18_II_S	0.947	0.947	1.021	0.947	1.021	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
SSTL18_I_F	0.947	0.947	1.021	0.947	1.021	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
SSTL18_I_S	0.947	0.947	1.021	0.947	1.021	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
SUB_LVDS	1.002	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T_{PW}(1)	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Table 103: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.0}$	Total jitter(3)(4)	4.0 Gb/s	–	–	0.32	UI
$D_{J4.0}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI

Table 105: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(1)	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(2)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(2)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI(2)	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort(2)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:

1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

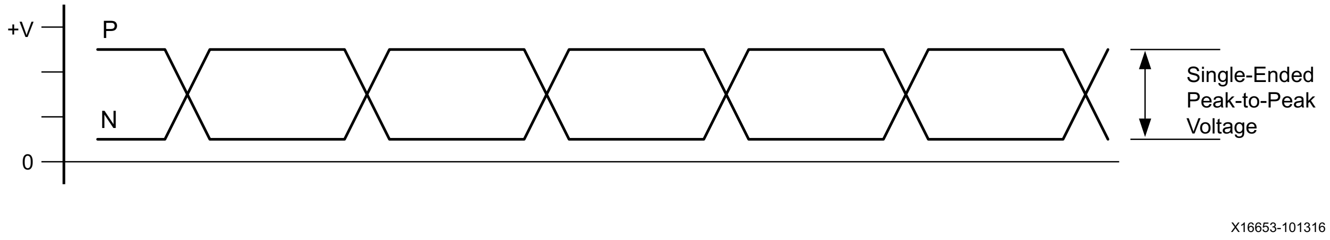

Figure 5: **Single-Ended Peak-to-Peak Voltage**

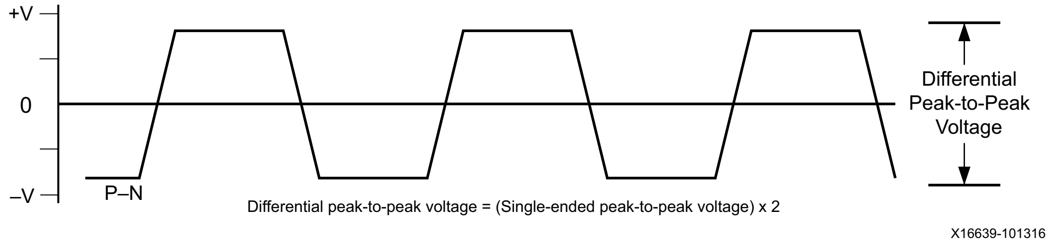

Figure 6: **Differential Peak-to-Peak Voltage**

Table 107 and Table 108 summarize the DC specifications of the clock input of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further details.

Table 107: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 108: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

Table 117: **GTY Transceiver Protocol List** ***(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: –2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: –2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: –2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: –2E, -2I, -1E, -1I Added -2E (V_{CCINT} = 0.85V) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{RFPSCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the *PS NAND Memory Controller Interface* section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU\_REF\_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the PS-GTR Transceiver section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90,and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPPOUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPPOUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the Integrated Interface Block for Interlaken and Integrated Interface Block for 100G Ethernet MAC and PCS sections. Revised the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3.