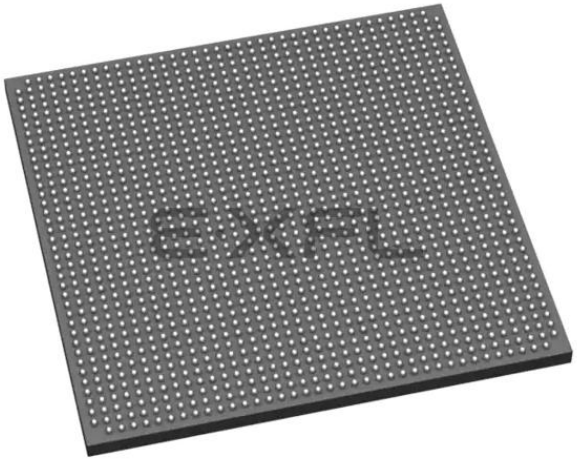
AMD Xilinx - XCZU19EG-L1FFVB1517I Datasheet



Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Quad ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™, ARM Mali™-400 MP2
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 600MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 1143K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu19eg-l1ffvb1517i

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{CCO}(8)	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(9)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(10)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(11)	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$(12)	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(12)	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$(12)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$(12)	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V_{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 4: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **PS MIO Pull-up and Pull-down Current**

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 3.3V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 2.5V.	20	80	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO_PSMIO} = 1.8V.	15	65	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 2.5V.	20	80	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	15	65	µA

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks(1)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	100%	–0.40	78%
V_{CCO} + 0.45	100%	–0.45	40%
V_{CCO} + 0.50	100%	–0.50	24%
V_{CCO} + 0.55	100%	–0.55	18.0%
V_{CCO} + 0.60	100%	–0.60	13.0%
V_{CCO} + 0.65	100%	–0.65	10.8%
V_{CCO} + 0.70	92%	–0.70	9.0%
V_{CCO} + 0.75	92%	–0.75	7.0%
V_{CCO} + 0.80	92%	–0.80	6.0%
V_{CCO} + 0.85	92%	–0.85	5.0%
V_{CCO} + 0.90	92%	–0.90	4.0%
V_{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	100%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 17: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{ILHS}(3)	V_{IHHS}(3)	V_{OCM}(V)(4)			V_{OD}(V)(5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS(8)	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(9)	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 23.
7. LVDS is specified in Table 24.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU5EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU6CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU6EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU7CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU9CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU9EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)

Table 42: **Linear Quad-SPI Interface(1)**

Symbol	Description	Load Conditions(2)	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK5}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK5}$	Slave select asserted to next clock edge.(3)	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS5}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO5}$	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK5}$	Setup time, all inputs.	15 pF	2.4	–	ns
		30 pF	2.4	–	ns
$T_{QSPICKD5}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK5}$	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
$F_{QSPICLK5}$	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. $T_{QSPISSSCLK5}$ is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: **ULPI Interface(1)**

Symbol	Description	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs.	4.5	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs.	0	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs.	2.0	8.86	ns
$F_{ULPICLK}$	ULPI reference clock frequency.	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS SPI Controller Interface

Table 48: **SPI Interfaces**(1)

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: **CAN Interface**(1)

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Programmable Logic (PL) Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Zynq UltraScale+ MPSoC. These values are subject to the same guidelines as the AC Switching Characteristics, page 22. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 70: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 71: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3(3)		-2(3)		-1		-2(3)		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(4)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(4)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_F_{VCOMIN}/2.
3. In the SBVA484 package, the maximum data rate is 1260 Mb/s for DDR interfaces and 630 Mb/s for SDR interfaces.
4. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: **IOB High Density (HD) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

IOB High Performance (HP) Switching Characteristics

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS18_F_8	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.600	0.573	0.600	0.733	0.733	0.767	0.733	0.767	ns
LVCMOS18_M_12	0.418	0.418	0.445	0.418	0.445	0.640	0.640	0.678	0.640	0.678	0.670	0.670	0.709	0.670	0.709	ns
LVCMOS18_M_2	0.418	0.418	0.445	0.418	0.445	0.798	0.798	0.822	0.798	0.822	0.991	0.991	1.016	0.991	1.016	ns
LVCMOS18_M_4	0.418	0.418	0.445	0.418	0.445	0.664	0.664	0.693	0.664	0.693	0.798	0.798	0.836	0.798	0.836	ns
LVCMOS18_M_6	0.418	0.418	0.445	0.418	0.445	0.629	0.629	0.663	0.629	0.663	0.735	0.735	0.775	0.735	0.775	ns
LVCMOS18_M_8	0.418	0.418	0.445	0.418	0.445	0.626	0.626	0.661	0.626	0.661	0.705	0.705	0.746	0.705	0.746	ns
LVCMOS18_S_12	0.418	0.418	0.445	0.418	0.445	0.795	0.795	0.861	0.795	0.861	0.683	0.683	0.721	0.683	0.721	ns
LVCMOS18_S_2	0.418	0.418	0.445	0.418	0.445	0.862	0.862	0.897	0.862	0.897	1.076	1.076	1.098	1.076	1.098	ns
LVCMOS18_S_4	0.418	0.418	0.445	0.418	0.445	0.716	0.716	0.758	0.716	0.758	0.829	0.829	0.872	0.829	0.872	ns
LVCMOS18_S_6	0.418	0.418	0.445	0.418	0.445	0.682	0.682	0.724	0.682	0.724	0.724	0.724	0.762	0.724	0.762	ns
LVCMOS18_S_8	0.418	0.418	0.445	0.418	0.445	0.707	0.707	0.760	0.707	0.760	0.709	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.462	0.426	0.426	0.443	0.426	0.443	0.548	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.462	0.553	0.553	0.582	0.553	0.582	0.645	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.462	0.749	0.749	0.803	0.749	0.803	0.821	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.447	0.441	0.441	0.459	0.441	0.459	0.560	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.447	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.447	0.760	0.760	0.818	0.760	0.818	0.837	0.837	0.899	0.837	0.899	ns
LVDS	0.539	0.539	0.620	0.539	0.620	0.626	0.626	0.662	0.626	0.662	960.447	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.415	0.502	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	8.792	0.914	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.407	0.430	0.407	0.430	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.407	0.430	0.407	0.430	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.407	0.430	0.407	0.430	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.409	0.431	0.409	0.431	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.431	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.431	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.409	0.431	0.409	0.431	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.409	0.431	0.409	0.431	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.409	0.431	0.409	0.431	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.399	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.399	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.399	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns

Table 85: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 91: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
				-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
$T_{PSMMCMCC\_ZU2}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU2}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU3}$		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
$T_{PHMMCMCC\_ZU3}$		Hold			–0.19	–0.19	0.13	0.13	ns
$T_{PSMMCMCC\_ZU4}$		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU4}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU5}$		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
$T_{PHMMCMCC\_ZU5}$		Hold		–0.12	–0.12	–0.12	0.27	0.48	ns
$T_{PSMMCMCC\_ZU6}$		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU6}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU7}$		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
$T_{PHMMCMCC\_ZU7}$		Hold		–0.14	–0.14	–0.14	0.37	0.38	ns
$T_{PSMMCMCC\_ZU9}$		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU9}$		Hold		–0.11	–0.11	–0.11	0.16	0.18	ns
$T_{PSMMCMCC\_ZU11}$		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
$T_{PHMMCMCC\_ZU11}$		Hold		–0.08	–0.08	0.04	0.35	0.74	ns
$T_{PSMMCMCC\_ZU15}$		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
$T_{PHMMCMCC\_ZU15}$		Hold		–0.10	–0.10	–0.10	0.17	0.19	ns
$T_{PSMMCMCC\_ZU17}$		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU17}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns
$T_{PSMMCMCC\_ZU19}$		Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns
$T_{PHMMCMCC\_ZU19}$		Hold		–0.16	–0.16	–0.16	0.31	0.34	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 99: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 100: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$[(1)(2)]	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$[(1)(2)]	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 101: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 102: **GTH Transceiver User Clock Switching Characteristics[(1)]**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[(2)]	-2[(2)(3)]	-1[(4)(5)]	-2[(3)]	-1[(5)]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz

Table 113: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 114: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3(2)	-2(2)(3)	-1(4)(5)	-2(3)	-1(5)	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK(6) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 117. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(2)	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(3)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(3)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 118).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 119).
- 12 x 25.78125 Gb/s lane logic only mode (Table 120).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 109 for the F_{GTYMAX} description.

Table 118: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.