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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 103K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	484-BFBGA, FCBGA
Supplier Device Package	484-FCBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu2cg-1sbva484e

Recommended Operating Conditions

 Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
Processor System					
$V_{CC_PSINTFP}$ ⁽³⁾	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
$V_{CC_PSINTFP_DDR}$ ⁽³⁾	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
$V_{PS_MGTRAVCC}$	PS-GTR supply voltage.	0.825	0.850	0.875	V
$V_{PS_MGTRAVTT}$	PS-GTR termination voltage.	1.746	1.800	1.854	V
V_{CCO_PSDDR} ⁽⁴⁾	PS DDR I/O supply voltage.	1.06	–	1.575	V
$V_{CC_PSDDR_PLL}$	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V_{CCO_PSIO} ⁽⁵⁾	PS I/O supply.	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage.	–0.200	–	$V_{CCO_PSIO} + 0.200$	V
	PS DDR I/O input voltage.	–0.200	–	$V_{CCO_PSDDR} + 0.200$	
V_{CC_PSBATT} ⁽⁶⁾	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	1.200	–	1.500	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO} ⁽⁷⁾	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE ($V_{CCINT} = 0.72V$) devices: PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V

Quiescent Supply Current

Table 9: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCINTQ}	Quiescent V _{CCINT} supply current.	XCZU2	N/A	393	393	344	344	mA
		XCZU3	N/A	393	393	344	344	mA
		XCZU4	719	684	684	601	601	mA
		XCZU5	719	684	684	601	601	mA
		XCZU6	1629	1549	1549	1358	1358	mA
		XCZU7	1263	1201	1201	1055	1055	mA
		XCZU9	1629	1549	1549	1358	1358	mA
		XCZU11	1786	1699	1699	1491	1491	mA
		XCZU15	1987	1890	1890	1660	1660	mA
		XCZU17	2728	2594	2594	2275	2275	mA
		XCZU19	2728	2594	2594	2275	2275	mA
I _{CCINT_IOQ}	Quiescent V _{CCINT_IO} supply current.	XCZU2	N/A	44	44	44	44	mA
		XCZU3	N/A	44	44	44	44	mA
		XCZU4	61	59	59	59	59	mA
		XCZU5	61	59	59	59	59	mA
		XCZU6	61	59	59	59	59	mA
		XCZU7	120	115	115	115	115	mA
		XCZU9	61	59	59	59	59	mA
		XCZU11	120	115	115	115	115	mA
		XCZU15	61	59	59	59	59	mA
		XCZU17	164	158	158	158	158	mA
		XCZU19	164	158	158	158	158	mA
I _{CCOQ}	Quiescent V _{CCO} supply current.	All devices	1	1	1	1	1	mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current.	XCZU2	N/A	55	55	55	55	mA
		XCZU3	N/A	55	55	55	55	mA
		XCZU4	90	90	90	90	90	mA
		XCZU5	90	90	90	90	90	mA
		XCZU6	227	227	227	227	227	mA
		XCZU7	174	174	174	174	174	mA
		XCZU9	227	227	227	227	227	mA
		XCZU11	255	255	255	255	255	mA
		XCZU15	266	266	266	266	266	mA
		XCZU17	396	396	396	396	396	mA
		XCZU19	396	396	396	396	396	mA

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

Power Supply Requirements

Table 10 shows the minimum current, in addition to I_{CCQ} maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 10: Power-on Current by Device⁽¹⁾

I_{CC} Min =	I_{CCQ} +	XCZU2	XCZU3	XCZU4	XCZU5	XCZU6	XCZU7	XCZU9	XCZU11	XCZU15	XCZU17	XCZU19	Units
$I_{CCINTMIN}$	I_{CCINTQ}^+	464	464	770	770	1800	1514	1800	1961	2242	3433	3433	mA
$I_{CCINT_IOMIN}^+$ $I_{CCBRAMMIN}$	$I_{CCBRAMQ}^+$ $I_{CCINT_IOQ}^+$	155	155	257	257	600	505	600	654	748	1145	1145	mA
I_{CCOMIN}	I_{CCOQ}^+	50	50	50	50	50	50	50	55	63	96	96	mA
$I_{CCAUXMIN}^+$ I_{CCAUX_IOMIN}	I_{CCAUXQ}^+ $I_{CCAUX_IOQ}^+$	111	111	386	386	650	362	650	709	810	1240	1240	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

Table 11: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT} .	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO} .	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU} .	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO} .	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX} .	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM} .	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms
$T_{VCC_PSINTFP}$	Ramp time from GND to 95% of $V_{CC_PSINTFP}$.	0.2	40	ms
$T_{VCC_PSINTLP}$	Ramp time from GND to 95% of $V_{CC_PSINTLP}$.	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX} .	0.2	40	ms
$T_{VCC_PSINTFP_DDR}$	Ramp time from GND to 95% of $V_{CC_PSINTFP_DDR}$.	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC} .	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL} .	0.2	40	ms
$T_{PS_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC_MGTRAVCC}$.	0.2	40	ms
$T_{PS_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC_MGTRAVTT}$.	0.2	40	ms

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 25](#).

Table 25: Speed Specification Version By Device

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 26](#) correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See [Table 3](#) for operating voltages listed by speed grade.

Table 26: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU2EG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU3CG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU3EG	-2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) -1LI ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.72V$)		-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCZU4CG	-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU4EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU4EV	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU5CG	-2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		

Table 26: Speed Grade Designations by Device (Cont'd)

Device	Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU5EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU5EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU6CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU6EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU7CG	-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU9CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU9EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)

Processor System (PS) Performance Characteristics

Table 28: Processor Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F _{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F _{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: Configuration and Security Unit Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{CSUCIBMAX}	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: PS DDR Performance

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁵⁾	664	2400	664	2400	664	2400	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package ⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package ⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s

Table 61: PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
PLL _{REFCLKMASK}	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
1 MHz		–	–	–138		
PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz	
	1 KHz	–	–	–108		
	10 KHz	–	–	–116		
	100 KHz	–	–	–123		
	1 MHz	–	–	–136		
		10 MHz	–	–	–138	

Notes:

- For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: PS-GTR Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T _{RTX}	TX rise time.	20%–80%	–	65	–	ps
T _{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 67: USB 3.0 Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: Serial-GMII Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: PS SYSMON Specifications

Parameter	Comments	Conditions	Min	Typ	Max	Units
$V_{CC_PSADC} = 1.8V \pm 3\%$, $T_j = -40^\circ C$ to $100^\circ C$, typical values at $T_j = 40^\circ C$						
ADC Accuracy ($T_j = -55^\circ C$ to $125^\circ C$) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		$T_j = -55^\circ C$ to $110^\circ C$	–	–	± 3.5	$^\circ C$
		$T_j = 110^\circ C$ to $125^\circ C$	–	–	± 5	$^\circ C$
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 2.5	%

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

Table 102: GTH Transceiver User Clock Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{TXIN2}	TXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
F _{RXIN2}	RXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
$T_{J16.375}$	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J15.0}$	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J14.1}$	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J14.1}$	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J13.1}$	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J12.5_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J12.5_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
$T_{J11.3_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J10.3125_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J10.3125_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
$T_{J9.953_QPLL}$	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953_QPLL}$	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
$T_{J9.953_CPLL}$	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953_CPLL}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
$T_{J8.0}$	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
$T_{J6.6}$	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
$T_{J5.0}$	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
$T_{J4.25}$	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
$T_{J4.0}$	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
$D_{J4.0}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
$T_{J3.20}$	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 104: GTH Transceiver Receiver Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 105](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide (UG578)* for further information.

Table 109: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTymax}	GTY maximum line rate		32.75		28.21				25.7813				Gb/s
F _{GTymin}	GTY minimum line rate		0.5		0.5				0.5				Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyCRANGE}	CPLL line rate range ⁽¹⁾	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyQRANGE1}	QPLL0 line rate range ⁽²⁾	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTyQRANGE2}	QPLL1 line rate range ⁽³⁾	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 115: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 116: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)		–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance⁽²⁾						
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s	0.25	–	–	UI
J _{T_SJ28.21}	Sinusoidal jitter (QPLL) ⁽³⁾	28.21 Gb/s	0.30	–	–	UI
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ8.0}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI
J _{T_SJ6.6}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

Table 117: GTY Transceiver Protocol List (Cont'd)

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant ⁽³⁾
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale+ Integrated 100G Ethernet MAC/PCS](#). The *UltraScale Architecture and Product Overview (DS890)* lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 121: Maximum Performance for 100G Ethernet Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2 ⁽¹⁾	-1	-2	-1 ⁽²⁾	
F _{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V_{CCINT}=0.72V.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *UltraScale Architecture and Product Overview (DS890)* lists the Zynq UltraScale+ MPSoCs that include this block.

Table 122: Maximum Performance for PCI Express Designs⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{CORECLK}	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{MCAPCLK}	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Configuration Switching Characteristics

Table 127: Configuration Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T _{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T _{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
T _{PS_PROG_B}	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F _{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F _{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
F _{CFGMCLK}	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
F _{CFGMCLKTOL}	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T _{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max