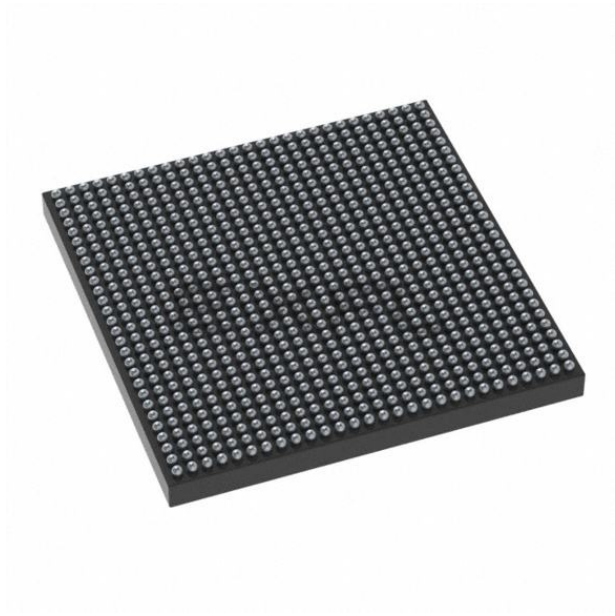

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 103K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu2cg-2sfvc784i

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTLP}$
2. V_{CC_PSAUX}, V_{CC_PSADC}, and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC\_PSINTFP}$ and $V_{CC\_PSINTFP\_DDR}$ driven from the same supply source.
2. $V_{PS\_MGTRAVCC}$ and $V_{CC\_PSDDR\_PLL}$ in any order or simultaneously.
3. $V_{PS\_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

PL I/O Levels

Table 14: **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL135_II	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL15_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.0	–8.0
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 19: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks(1)**

I/O Standard	V_{ICM} (V)(2)			V_{ID} (V)(3)		V_{OL} (V)(4)	V_{OH} (V)(5)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	($V_{CCO}/2$) – 0.120	$V_{CCO}/2$	($V_{CCO}/2$) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	8.0	–8.0
DIFF_SSTL135	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	9.0	–9.0
DIFF_SSTL15	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.175	($V_{CCO}/2$) + 0.175	10.0	–10.0
DIFF_SSTL18_I	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.470	($V_{CCO}/2$) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: **Table 21 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU2CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU2EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU4CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

Table 60: **PS-GTR Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequencies supported.	PCI Express	100 MHz			
		SATA	125 MHz or 150 MHz			
		USB 3.0	26 MHz, 52 MHz, or 100 MHz			
		DisplayPort	27 MHz, 108 MHz, or 135 MHz			
		SGMII	125 MHz			
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only.	40	–	60	%
		USB 3.0 with reference clock <40 MHz.	47.5	–	52.5	%

Table 67: **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: **PS SYSMON Specifications**

Parameter	Comments	Conditions	Min	Typ	Max	Units
V_{CC_PSADC} = 1.8V ±3%, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy (T_j = –55°C to 125°C) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		T_j = –55°C to 110°C	–	–	±3.5	°C
		T_j = 110°C to 125°C	–	–	±5	°C
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC}.	T_j = –40°C to 125°C	–	–	±1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	T_j = –40°C to 125°C	–	–	±2.5	%

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Table 75: **IOB High Density (HD) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS33_S_8	1.154	1.154	1.213	1.154	1.213	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
LVDS_25	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	1.003	1.003	1.116	1.003	1.116	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTL_F_12	1.164	1.164	1.223	1.164	1.223	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVTTL_F_16	1.164	1.164	1.223	1.164	1.223	2.464	2.464	2.732	2.464	2.732	1.750	1.750	1.986	1.750	1.986	ns
LVTTL_F_4	1.164	1.164	1.223	1.164	1.223	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVTTL_F_8	1.164	1.164	1.223	1.164	1.223	2.582	2.582	2.787	2.582	2.787	1.910	1.910	2.063	1.910	2.063	ns
LVTTL_S_12	1.164	1.164	1.223	1.164	1.223	2.731	2.731	3.075	2.731	3.075	2.072	2.072	2.343	2.072	2.343	ns
LVTTL_S_16	1.164	1.164	1.223	1.164	1.223	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVTTL_S_4	1.164	1.164	1.223	1.164	1.223	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns
LVTTL_S_8	1.164	1.164	1.223	1.164	1.223	2.929	2.929	3.260	2.929	3.260	2.260	2.260	2.532	2.260	2.532	ns
SLVS_400_25	1.020	1.020	1.136	1.020	1.136	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.780	0.780	0.867	0.780	0.867	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
SSTL12_S	0.780	0.780	0.867	0.780	0.867	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
SSTL135_F	0.798	0.798	0.881	0.798	0.881	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
SSTL135_II_F	0.798	0.798	0.881	0.798	0.881	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
SSTL135_II_S	0.798	0.798	0.881	0.798	0.881	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
SSTL135_S	0.798	0.798	0.881	0.798	0.881	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
SSTL15_F	0.838	0.838	0.880	0.838	0.880	1.612	1.612	1.754	1.612	1.754	1.357	1.357	1.464	1.357	1.464	ns
SSTL15_II_F	0.838	0.838	0.880	0.838	0.880	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
SSTL15_II_S	0.838	0.838	0.880	0.838	0.880	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
SSTL15_S	0.838	0.838	0.880	0.838	0.880	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
SSTL18_II_F	0.947	0.947	1.021	0.947	1.021	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
SSTL18_II_S	0.947	0.947	1.021	0.947	1.021	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
SSTL18_I_F	0.947	0.947	1.021	0.947	1.021	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
SSTL18_I_S	0.947	0.947	1.021	0.947	1.021	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
SUB_LVDS	1.002	1.002	1.036	1.002	1.036	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Table 78: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

DSP48 Slice Switching Characteristics

Table 83: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F_{MAX}	With all registers used.	891	775	645	644	600	MHz
F_{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG.	635	544	456	440	413	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG.	655	565	468	453	423	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 84: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$MMCM\_F_{INMAX}$	Maximum input clock frequency.	1066	933	800	933	800	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency.	10	10	10	10	10	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
$MMCM\_F_{INDUTY}$	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter.	Note 3					
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
$MMCM\_T_{LOCKMAX}$	MMCM maximum lock time for $MMCM\_F_{PFDMIN}$.	100	100	100	100	100	µs
$MMCM\_F_{OUTMAX}$	MMCM maximum output frequency.	891	775	667	725	667	MHz
$MMCM\_F_{OUTMIN}$	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	6.25	MHz
$MMCM\_T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
$MMCM\_RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
$MMCM\_F_{PFDMIN}$	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
$MMCM\_T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 109: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range(1)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range(2)	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range(3)	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 115: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 116: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 117: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Video Codec Performance

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 123: **VCU Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 124: **PL SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity(2)	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic (T_j = –55°C to 125°C)	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: –2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: –2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: –2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: –2E, -2I, -1E, -1I Added -2E (V_{CCINT} = 0.85V) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{RFPSCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the *PS NAND Memory Controller Interface* section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU\_REF\_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the PS-GTR Transceiver section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90,and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPPOUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPPOUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the Integrated Interface Block for Interlaken and Integrated Interface Block for 100G Ethernet MAC and PCS sections. Revised the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1. Updated Table 2, Table 4, Table 6, Table 7, and Table 9. Revised the Power Supply Sequencing section including Table 10. Added PS and VCU ramp times to Table 11. Revised V_{ODIFF} in Table 24. Updated Table 25. Added Note 1 to Table 26. Table 30 replaces the previous three PS memory performance tables. Added values to Table 34, Table 37, and Table 38. Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the *PS NAND Memory Controller Interface* section. Added and updated data in Table 40. Added Note 3 to Table 41. Added Note 3 to Table 42. Added Note 1 to Table 45. Updated Table 48 and removed Note 3. Added data to Table 56. Updated Table 60. Added Table 61. Updated Table 63. Revised Table 69. Added data to Table 70. Added Note 2 to Table 71. Updated Table 74 and added Note 4. Updated V_L and V_H values in Table 78. Added T_{MINPER_CLK}, revised F_{REFCLK}, and Note 1 to Table 82. Added MMCM_F_{DPRCLK_MAX} to Table 85 and PLL_F_{DPRCLK_MAX} to Table 86. Added data to Table 94, Table 96, Table 98, Table 101, and updated the note references in Table 102. Updated Table 103 and added Note 8. Updated Table 104 and added Note 7. Added more protocols, Note 1 and Note 2 to Table 105. Removed the *GTH Transceiver Protocol Jitter Characteristics* section because it is covered in Table 105. Added Note 1 to Table 109. Added data to Table 106, Table 108, Table 110, Table 113. Added Note 2 to Table 112. Added note references in Table 114. Updated Table 115 and added Note 8. Updated Table 116 and added Note 7. Added more protocols and Note 3 to Table 117. Removed the *GTY Transceiver Protocol Jitter Characteristics* section because it is covered in Table 117. Revised Table 124. Added T_{POR} and updated F_{ICAPCK} in Table 127. Updated the Automotive Applications Disclaimer.
06/20/2016	1.1	Updated the Summary description. In Table 1, revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU}, I_{RPD}, and Note 4 to Table 2 and updated $V_{PS\_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 4. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 14, Table 15, and Table 17. Updated Table 23, including removing the V_{CCO} specification and adding Note 1. Added Note 1 to Table 24. Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28. Updated the -2 value in Table 29. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33. Added VCO frequencies to Table 36. Added the T_{PSPOR} minimum to Table 37 and updated Note 1. Added Table 38. Added value delineation over V_{CCINT} operating voltages in Table 39. Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the *PS NAND Memory Controller Interface* section. Revised some units and Note 1 in Table 41 and Table 42. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43. Added $F_{TSI\_REF\_CLK}$ to Table 44 and updated Note 1. In Table 45, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 46, revised Note 1. In Table 47, revised Note 1. Revised Table 48, including Note 1, and added Note 2 and Note 3. In Table 49, Table 50, Table 51, and Table 53, revised Note 1. Updated Table 71. Replaced Table 74. Updated Table 75 and Table 76. Updated Table 78 and Table 79. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97. Added Table 100 and Table 112. Added Note 2 to Table 106. Revised data in Table 109. Revised Table 114. Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121. Moved Table 123. Revised INL in Table 124. Added notes to Table 125 and Table 126. In the *eFUSE and Programming Conditions* table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.