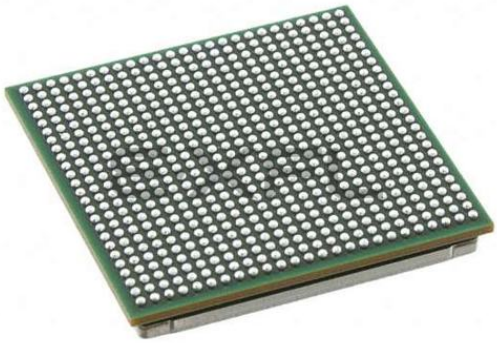

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 103K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	625-BFBGA, FCBGA
Supplier Device Package	625-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu2cg-l2sfva625e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
Processor System					
$V_{CC\_PSINTFP}$(3)	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V_{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
$V_{CC\_PSINTFP\_DDR}$(3)	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V_{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V_{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
$V_{PS\_MGTRAVCC}$	PS-GTR supply voltage.	0.825	0.850	0.875	V
$V_{PS\_MGTRAVTT}$	PS-GTR termination voltage.	1.746	1.800	1.854	V
V_{CCO_PSDDR}(4)	PS DDR I/O supply voltage.	1.06	–	1.575	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V_{CCO_PSIO}(5)	PS I/O supply.	1.710	–	3.465	V
V_{PSIN}	PS I/O input voltage.	–0.200	–	V_{CCO_PSIO} + 0.200	V
	PS DDR I/O input voltage.	–0.200	–	V_{CCO_PSDDR} + 0.200	
V_{CC_PSBATT}(6)	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	1.200	–	1.500	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(7)	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V

Table 17: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{ILHS}(3)	V_{IHHS}(3)	V_{OCM}(V)(4)			V_{OD}(V)(5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS(8)	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–	–	–
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(9)	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 23.
7. LVDS is specified in Table 24.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 18: **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL135_II	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL15_II	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU11EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU17EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCZU2CG	N/A	Vivado tools 2017.1 v1.10					
XCZU2EG	N/A	Vivado tools 2017.1 v1.10					
XCZU3CG	N/A	Vivado tools 2017.1 v1.10					
XCZU3EG	N/A	Vivado tools 2017.1 v1.10					
XCZU4CG	N/A						
XCZU4EG							
XCZU4EV							
XCZU5CG	N/A						
XCZU5EG							
XCZU5EV							
XCZU6CG	N/A	Vivado tools 2017.1 v1.10					
XCZU6EG		Vivado tools 2017.1 v1.10					
XCZU7CG	N/A						
XCZU7EG							
XCZU7EV							
XCZU9CG	N/A	Vivado tools 2017.1 v1.10					
XCZU9EG		Vivado tools 2017.1 v1.10					
XCZU11EG							
XCZU15EG							
XCZU17EG							
XCZU19EG							

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Processor System (PS) Performance Characteristics

Table 28: **Processor Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F_{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F_{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: **Configuration and Security Unit Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{CSUCIBMAX}$	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: **PS DDR Performance**

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM(1)(2)	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM(1)(3)	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM(1)(2)	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM(1)(3)	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM(1)(2)	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM(1)(3)	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package(5)	664	2400	664	2400	664	2400	Mb/s
		Dual die package(4)(5)	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package(5)	664	2133	664	2133	664	2133	Mb/s
		Dual die package(4)(5)	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package(5)	664	1066	664	1066	664	1066	Mb/s
		Dual die package(4)(5)	664	1066	664	1066	664	1066	Mb/s

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**(1)

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

Table 37: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time.(1)	10	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time.	3	–	–	PS_REF_CLK Clock Cycles

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: **PS Clocks Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{TOPSW\_MAINMAX}$	TOPSW_MAIN maximum frequency.	600	533	533	MHz
$F_{TOPSW\_LSBUSMAX}$	TOPSW_LSBUS maximum frequency.	100	100	100	MHz
$F_{GDMAMAX}$	FPD-DMA maximum frequency.	600	600	600	MHz
$F_{DPDMAMAX}$	DisplayPort DMA maximum frequency.	600	600	600	MHz
$F_{LPD\_SWITCH\_CTRLMAX}$	LPD_SWITCH_CTRL maximum frequency.	600	500	500	MHz
$F_{LPD\_LSBUS\_CTRLMAX}$	LPD_LSBUS_CTRL maximum frequency.	100	100	100	MHz
$F_{ADMAMAX}$	LPD-DMA maximum frequency.	600	500	500	MHz
$F_{APLL\_TO\_LPDMAX}$	APLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{DPLL\_TO\_LPDMAX}$	DPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{VPLL\_TO\_LPDMAX}$	VPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{IOPLL\_TO\_LPDMAX}$	IOPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{RPLL\_TO\_FPDMAX}$	RPLL_TO_FPD maximum frequency.	533	533	533	MHz

Table 45: **SD/SDIO Interface(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
$F_{SDSDRCLK2}$	SDR50 mode device clock frequency.	–	100	MHz
	SDR25 mode device clock frequency.	–	50	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs.	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs.	24.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle.	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs.(2)	2.2	13.8	ns
$T_{SDHSDIVW}$	Input valid data window.(3)	0.35	–	UI
$F_{SDHSCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle.	45	55	%
T_{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs.	2.0	–	ns
$F_{SDIDCLK}$	Clock frequency in identification mode.	–	400	KHz
F_{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS I2C Controller Interface

Table 47: **I2C Interface(1)**

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µs
$T_{I2CSCKH}$	SCL High time.	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 61: **PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$PLL_{REFCLKMASK}$	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
		10 MHz	–	–	–148	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
		10 MHz	–	–	–142	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
		1 MHz	–	–	–138	
		10 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz
		1 KHz	–	–	–108	
		10 KHz	–	–	–116	
		100 KHz	–	–	–123	
		1 MHz	–	–	–136	
		10 MHz	–	–	–138	

Notes:

1. For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: **PS-GTR Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T_{RTX}	TX rise time.	20%–80%	–	65	–	ps
T_{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
LVCMOS18_F_8	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.600	0.573	0.600	0.733	0.733	0.767	0.733	0.767	ns
LVCMOS18_M_12	0.418	0.418	0.445	0.418	0.445	0.640	0.640	0.678	0.640	0.678	0.670	0.670	0.709	0.670	0.709	ns
LVCMOS18_M_2	0.418	0.418	0.445	0.418	0.445	0.798	0.798	0.822	0.798	0.822	0.991	0.991	1.016	0.991	1.016	ns
LVCMOS18_M_4	0.418	0.418	0.445	0.418	0.445	0.664	0.664	0.693	0.664	0.693	0.798	0.798	0.836	0.798	0.836	ns
LVCMOS18_M_6	0.418	0.418	0.445	0.418	0.445	0.629	0.629	0.663	0.629	0.663	0.735	0.735	0.775	0.735	0.775	ns
LVCMOS18_M_8	0.418	0.418	0.445	0.418	0.445	0.626	0.626	0.661	0.626	0.661	0.705	0.705	0.746	0.705	0.746	ns
LVCMOS18_S_12	0.418	0.418	0.445	0.418	0.445	0.795	0.795	0.861	0.795	0.861	0.683	0.683	0.721	0.683	0.721	ns
LVCMOS18_S_2	0.418	0.418	0.445	0.418	0.445	0.862	0.862	0.897	0.862	0.897	1.076	1.076	1.098	1.076	1.098	ns
LVCMOS18_S_4	0.418	0.418	0.445	0.418	0.445	0.716	0.716	0.758	0.716	0.758	0.829	0.829	0.872	0.829	0.872	ns
LVCMOS18_S_6	0.418	0.418	0.445	0.418	0.445	0.682	0.682	0.724	0.682	0.724	0.724	0.724	0.762	0.724	0.762	ns
LVCMOS18_S_8	0.418	0.418	0.445	0.418	0.445	0.707	0.707	0.760	0.707	0.760	0.709	0.709	0.745	0.709	0.745	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.462	0.426	0.426	0.443	0.426	0.443	0.548	0.548	0.581	0.548	0.581	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.462	0.553	0.553	0.582	0.553	0.582	0.645	0.645	0.685	0.645	0.685	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.462	0.749	0.749	0.803	0.749	0.803	0.821	0.821	0.890	0.821	0.890	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.447	0.441	0.441	0.459	0.441	0.459	0.560	0.560	0.589	0.560	0.589	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.447	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.447	0.760	0.760	0.818	0.760	0.818	0.837	0.837	0.899	0.837	0.899	ns
LVDS	0.539	0.539	0.620	0.539	0.620	0.626	0.626	0.662	0.626	0.662	960.447	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.415	0.502	0.502	0.522	0.502	0.522	N/A	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	8.792	0.914	0.914	0.937	0.914	0.937	N/A	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
POD10_F	0.407	0.407	0.430	0.407	0.430	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
POD10_M	0.407	0.407	0.430	0.407	0.430	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
POD10_S	0.407	0.407	0.430	0.407	0.430	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
POD12_DCI_F	0.409	0.409	0.431	0.409	0.431	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.431	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.431	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
POD12_F	0.409	0.409	0.431	0.409	0.431	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
POD12_M	0.409	0.409	0.431	0.409	0.431	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
POD12_S	0.409	0.409	0.431	0.409	0.431	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
SLVS_400_18	0.539	0.539	0.620	0.539	0.620	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.399	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.399	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.399	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 77: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

Table 79: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V_{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V_{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V_{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

MMCM Switching Characteristics

Table 85: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$MMCM\_F_{INMAX}$	Maximum input clock frequency.	1066	933	800	933	800	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency.	10	10	10	10	10	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
$MMCM\_F_{INDUTY}$	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter.	Note 3					
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	0.20	ns
$MMCM\_T_{LOCKMAX}$	MMCM maximum lock time for $MMCM\_F_{PFDMIN}$.	100	100	100	100	100	µs
$MMCM\_F_{OUTMAX}$	MMCM maximum output frequency.	891	775	667	725	667	MHz
$MMCM\_F_{OUTMIN}$	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	6.25	MHz
$MMCM\_T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
$MMCM\_RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
$MMCM\_F_{PFDMIN}$	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
$MMCM\_T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 93: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCZU2	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU3	SBVA484	105	ps
			SFVA625	108	ps
			SFVC784	93	ps
		XCZU4	SFVC784		ps
			FBVB900		ps
		XCZU5	SFVC784		ps
			FBVB900		ps
		XCZU6	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU7	FBVB900	141	ps
			FFVC1156	175	ps
			FFVF1517	305	ps
		XCZU9	FFVC900	119	ps
			FFVB1156	134	ps
		XCZU11	FFVC1156		ps
			FFVB1517		ps
			FFVF1517		ps
			FFVC1760	215	ps
		XCZU15	FFVC900	118	ps
			FFVB1156	132	ps
		XCZU17	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps
		XCZU19	FFVB1517	221	ps
			FFVC1760	226	ps
			FFVD1760	178	ps
			FFVE1924	174	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

Table 94 summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 94: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage.	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage.(1)	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor.(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 99: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 100: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$[(1)(2)]	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$[(1)(2)]	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 101: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 102: **GTH Transceiver User Clock Switching Characteristics[(1)]**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[(2)]	-2[(2)(3)]	-1[(4)(5)]	-2[(3)]	-1[(5)]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz

Table 102: **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 105: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(1)	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(2)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(2)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI(2)	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort(2)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:
1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale+ Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 118).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 119).
- 12 x 25.78125 Gb/s lane logic only mode (Table 120).

Zynq UltraScale+ MPSoCs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 109 for the F_{GTYMAX} description.

Table 118: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.