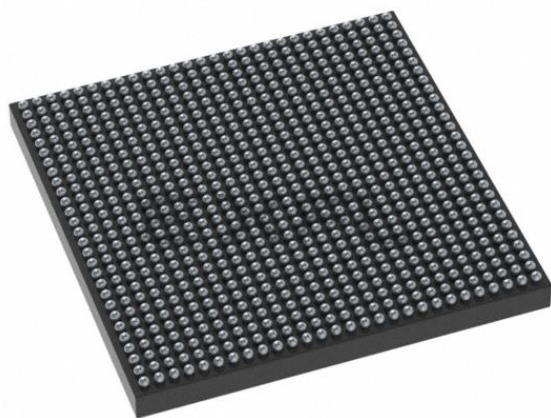




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 154K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu3cg-1sfvc784i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
V _{CCO} ⁽⁸⁾	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V _{CCAUX_IO} ⁽⁹⁾	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V _{IN} ⁽¹⁰⁾	I/O input voltage.	–0.200	–	V _{CCO} + 0.200	V
I _{IN} ⁽¹¹⁾	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
V _{MGTAVCC} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
V _{MGTAVTT} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
V _{MGTVCCAUX} ⁽¹²⁾	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
V _{MGTAVTTRCAL} ⁽¹²⁾	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V _{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 4: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
I_{CC_PSBATT} ⁽⁴⁾⁽⁵⁾	Battery supply current at $V_{CC_PSBATT} = 1.50V$, RTC enabled.	–	–	3650	nA
	Battery supply current at $V_{CC_PSBATT} = 1.50V$, RTC disabled.	–	–	650	nA
	Battery supply current at $V_{CC_PSBATT} = 1.20V$, RTC enabled.	–	–	3150	nA
	Battery supply current at $V_{CC_PSBATT} = 1.20V$, RTC disabled.	–	–	150	nA
I_{PSFS} ⁽⁶⁾	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
<i>Calibrated programmable on-die termination (DCI) in HP I/O banks⁽⁸⁾ (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{40}$.	–10% ⁽⁷⁾	40	+10% ⁽⁷⁾	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–10% ⁽⁷⁾	48	+10% ⁽⁷⁾	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{60}$.	–10% ⁽⁷⁾	60	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{40}$.	–10% ⁽⁷⁾	40	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{48}$.	–10% ⁽⁷⁾	48	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{60}$.	–10% ⁽⁷⁾	60	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{120}$.	–10% ⁽⁷⁾	120	+10% ⁽⁷⁾	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{240}$.	–10% ⁽⁷⁾	240	+10% ⁽⁷⁾	Ω
<i>Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{40}$.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{60}$.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{40}$.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{60}$.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{120}$.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where $ODT = RTT_{240}$.	–50%	240	+50%	Ω
<i>Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)</i>					
R ⁽⁹⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where $ODT = RTT_{48}$.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	$V_{CCO} \times 0.49$	$V_{CCO} \times 0.50$	$V_{CCO} \times 0.51$	V
	70% V_{CCO}	$V_{CCO} \times 0.69$	$V_{CCO} \times 0.70$	$V_{CCO} \times 0.71$	V

Table 4: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μ A.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
- If VRP resides at a different bank (DCI cascade), the range increases to $\pm 15\%$.
- VRP resistor tolerance is $(240\Omega \pm 1\%)$
- On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

Table 5: PS MIO Pull-up and Pull-down Current

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 3.3V$.	20	80	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 2.5V$.	20	80	μ A
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 1.8V$.	15	65	μ A
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$.	20	80	μ A
	Pad pull-down (when selected) at $V_{IN} = 2.5V$.	20	80	μ A
	Pad pull-down (when selected) at $V_{IN} = 1.8V$.	15	65	μ A

Table 11: Power Supply Ramp Time (Cont'd)

Symbol	Description	Min	Max	Units
$T_{V_{CCO_PSDDR}}$	Ramp time from GND to 95% of V_{CCO_PSDDR} .	0.2	40	ms
$T_{V_{CC_PSDDR_PLL}}$	Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$.	0.2	40	ms
$T_{V_{CCO_PSIO}}$	Ramp time from GND to 95% of V_{CCO_PSIO} .	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels⁽¹⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS33	-0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	-12
LVC MOS25	-0.300	0.700	1.700	$V_{CCO_PSIO} + 0.30$	0.70	1.70	12	-12
LVC MOS18	-0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	$V_{CCO_PSIO} + 0.30$	0.45	$V_{CCO_PSIO} - 0.45$	12	-12

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels⁽¹⁾

DDR Standard	V_{IL}		V_{IH}		$V_{OL}^{(2)}$	$V_{OH}^{(2)}$	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.8 \times V_{CCO_PSDDR} - 0.150$	$0.8 \times V_{CCO_PSDDR} + 0.150$	10	-0.1
LPDDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.3 \times V_{CCO_PSDDR} - 0.150$	$0.3 \times V_{CCO_PSDDR} + 0.150$	0.1	-10
DDR3	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.175$	$0.5 \times V_{CCO_PSDDR} + 0.175$	8	-8
LPDDR3	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8
DDR3L	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 23: LVDS_25 DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	100	350	600 ⁽²⁾	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 24: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		1.710	1.800	1.890	V
$V_{ODIFF}^{(2)}$	Differential output voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
$V_{OCM}^{(2)}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
$V_{IDIFF}^{(3)}$	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$		100	350	600 ⁽³⁾	mV
$V_{ICM_DC}^{(4)}$	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
$V_{ICM_AC}^{(5)}$	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

Processor System (PS) Performance Characteristics

Table 28: Processor Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F _{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F _{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: Configuration and Security Unit Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{CSUCIBMAX}	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: PS DDR Performance

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁵⁾	664	2400	664	2400	664	2400	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package ⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package ⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s

PS SPI Controller Interface

Table 48: SPI Interfaces⁽¹⁾

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: CAN Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	μs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	μs
$F_{CAN_REF_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 75: IOB High Density (HD) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	0.90V	0.85V	0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_F	0.856	0.856	0.900	0.856	0.900	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
HSTL_I_S	0.856	0.856	0.900	0.856	0.900	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
HSUL_12_F	0.780	0.780	0.867	0.780	0.867	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
HSUL_12_S	0.780	0.780	0.867	0.780	0.867	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
LVC MOS12_F_12	0.918	0.918	0.976	0.918	0.976	1.689	1.689	1.856	1.689	1.856	1.202	1.202	1.317	1.202	1.317	ns
LVC MOS12_F_4	0.918	0.918	0.976	0.918	0.976	1.742	1.742	1.922	1.742	1.922	1.353	1.353	1.478	1.353	1.478	ns
LVC MOS12_F_8	0.918	0.918	0.976	0.918	0.976	1.714	1.714	1.879	1.714	1.879	1.292	1.292	1.432	1.292	1.432	ns
LVC MOS12_S_12	0.918	0.918	0.976	0.918	0.976	2.073	2.073	2.247	2.073	2.247	1.581	1.581	1.717	1.581	1.717	ns
LVC MOS12_S_4	0.918	0.918	0.976	0.918	0.976	1.979	1.979	2.182	1.979	2.182	1.633	1.633	1.772	1.633	1.772	ns
LVC MOS12_S_8	0.918	0.918	0.976	0.918	0.976	2.205	2.205	2.406	2.205	2.406	1.767	1.767	1.928	1.767	1.928	ns
LVC MOS15_F_12	0.905	0.905	0.958	0.905	0.958	1.713	1.713	1.892	1.713	1.892	1.275	1.275	1.428	1.275	1.428	ns
LVC MOS15_F_16	0.905	0.905	0.958	0.905	0.958	1.722	1.722	1.881	1.722	1.881	1.260	1.260	1.407	1.260	1.407	ns
LVC MOS15_F_4	0.905	0.905	0.958	0.905	0.958	1.825	1.825	1.959	1.825	1.959	1.453	1.453	1.557	1.453	1.557	ns
LVC MOS15_F_8	0.905	0.905	0.958	0.905	0.958	1.778	1.778	1.930	1.778	1.930	1.378	1.378	1.458	1.378	1.458	ns
LVC MOS15_S_12	0.905	0.905	0.958	0.905	0.958	1.991	1.991	2.139	1.991	2.139	1.516	1.516	1.648	1.516	1.648	ns
LVC MOS15_S_16	0.905	0.905	0.958	0.905	0.958	2.172	2.172	2.389	2.172	2.389	1.707	1.707	1.888	1.707	1.888	ns
LVC MOS15_S_4	0.905	0.905	0.958	0.905	0.958	2.313	2.313	2.483	2.313	2.483	1.952	1.952	2.123	1.952	2.123	ns
LVC MOS15_S_8	0.905	0.905	0.958	0.905	0.958	2.170	2.170	2.400	2.170	2.400	1.817	1.817	1.984	1.817	1.984	ns
LVC MOS18_F_12	0.915	0.915	0.958	0.915	0.958	1.805	1.805	1.962	1.805	1.962	1.383	1.383	1.471	1.383	1.471	ns
LVC MOS18_F_16	0.915	0.915	0.958	0.915	0.958	1.785	1.785	1.917	1.785	1.917	1.338	1.338	1.446	1.338	1.446	ns
LVC MOS18_F_4	0.915	0.915	0.958	0.915	0.958	1.868	1.868	2.013	1.868	2.013	1.472	1.472	1.599	1.472	1.599	ns
LVC MOS18_F_8	0.915	0.915	0.958	0.915	0.958	1.797	1.797	1.979	1.797	1.979	1.384	1.384	1.487	1.384	1.487	ns
LVC MOS18_S_12	0.915	0.915	0.958	0.915	0.958	2.201	2.201	2.408	2.201	2.408	1.762	1.762	1.894	1.762	1.894	ns
LVC MOS18_S_16	0.915	0.915	0.958	0.915	0.958	2.173	2.173	2.362	2.173	2.362	1.702	1.702	1.834	1.702	1.834	ns
LVC MOS18_S_4	0.915	0.915	0.958	0.915	0.958	2.346	2.346	2.567	2.346	2.567	1.951	1.951	2.092	1.951	2.092	ns
LVC MOS18_S_8	0.915	0.915	0.958	0.915	0.958	2.292	2.292	2.511	2.292	2.511	1.848	1.848	2.008	1.848	2.008	ns
LVC MOS25_F_12	0.988	0.988	1.042	0.988	1.042	2.153	2.153	2.453	2.153	2.453	1.692	1.692	1.856	1.692	1.856	ns
LVC MOS25_F_16	0.988	0.988	1.042	0.988	1.042	2.105	2.105	2.406	2.105	2.406	1.623	1.623	1.786	1.623	1.786	ns
LVC MOS25_F_4	0.988	0.988	1.042	0.988	1.042	2.344	2.344	2.554	2.344	2.554	1.842	1.842	2.039	1.842	2.039	ns
LVC MOS25_F_8	0.988	0.988	1.042	0.988	1.042	2.184	2.184	2.516	2.184	2.516	1.726	1.726	1.910	1.726	1.910	ns
LVC MOS25_S_12	0.988	0.988	1.042	0.988	1.042	2.558	2.558	2.840	2.558	2.840	1.971	1.971	2.194	1.971	2.194	ns
LVC MOS25_S_16	0.988	0.988	1.042	0.988	1.042	2.449	2.449	2.740	2.449	2.740	1.852	1.852	2.063	1.852	2.063	ns
LVC MOS25_S_4	0.988	0.988	1.042	0.988	1.042	2.770	2.770	3.066	2.770	3.066	2.224	2.224	2.458	2.224	2.458	ns
LVC MOS25_S_8	0.988	0.988	1.042	0.988	1.042	2.663	2.663	2.963	2.663	2.963	2.091	2.091	2.373	2.091	2.373	ns
LVC MOS33_F_12	1.154	1.154	1.213	1.154	1.213	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVC MOS33_F_16	1.154	1.154	1.213	1.154	1.213	2.383	2.383	2.603	2.383	2.603	1.734	1.734	1.869	1.734	1.869	ns
LVC MOS33_F_4	1.154	1.154	1.213	1.154	1.213	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVC MOS33_F_8	1.154	1.154	1.213	1.154	1.213	2.603	2.603	2.822	2.603	2.822	1.937	1.937	2.130	1.937	2.130	ns
LVC MOS33_S_12	1.154	1.154	1.213	1.154	1.213	2.705	2.705	3.047	2.705	3.047	2.049	2.049	2.318	2.049	2.318	ns
LVC MOS33_S_16	1.154	1.154	1.213	1.154	1.213	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVC MOS33_S_4	1.154	1.154	1.213	1.154	1.213	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns

Table 79: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V _{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V _{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V _{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V _{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
POD10, 1.0V	POD10	50	0	V _{REF}	1.0
POD12, 1.2V	POD12	50	0	V _{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V _{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V _{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V _{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V _{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V _{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V _{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V _{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 ⁽²⁾	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 ⁽²⁾	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 ⁽²⁾	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F _{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T _{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

DSP48 Slice Switching Characteristics

Table 83: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	With all registers used.	891	775	645	644	600	MHz
F _{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	635	544	456	440	413	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG.	655	565	468	453	423	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 84: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F _{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F _{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F _{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 90](#) and [Table 91](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)									
T _{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	Setup	XCZU2	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU2}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU3}		Setup	XCZU3	N/A	2.27	2.37	2.55	2.64	ns
T _{PHFD_ZU3}		Hold			−0.36	−0.36	−0.14	−0.14	ns
T _{PSFD_ZU4}		Setup	XCZU4	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU4}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU5}		Setup	XCZU5	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU5}		Hold		−0.28	−0.28	−0.28	−0.09	−0.09	ns
T _{PSFD_ZU6}		Setup	XCZU6	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU6}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU7}		Setup	XCZU7	1.43	2.32	2.42	2.60	2.69	ns
T _{PHFD_ZU7}		Hold		−0.40	−0.40	−0.40	−0.21	−0.21	ns
T _{PSFD_ZU9}		Setup	XCZU9	0.96	1.79	1.86	1.93	2.02	ns
T _{PHFD_ZU9}		Hold		−0.05	−0.05	−0.05	0.27	0.42	ns
T _{PSFD_ZU11}		Setup	XCZU11	1.28	2.01	2.07	2.59	2.59	ns
T _{PHFD_ZU11}		Hold		−0.29	−0.29	−0.29	−0.09	0.19	ns
T _{PSFD_ZU15}		Setup	XCZU15	0.96	1.79	1.85	1.92	2.01	ns
T _{PHFD_ZU15}		Hold		−0.04	−0.04	−0.04	0.27	0.43	ns
T _{PSFD_ZU17}		Setup	XCZU17	1.41	2.29	2.38	2.57	2.65	ns
T _{PHFD_ZU17}		Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns
T _{PSFD_ZU19}	Setup	XCZU19	1.41	2.29	2.38	2.57	2.65	ns	
T _{PHFD_ZU19}	Hold		−0.38	−0.38	−0.38	−0.19	−0.19	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 97: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375 ⁽¹⁾		16.375 ⁽¹⁾		12.5		12.5		10.3125		Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽²⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽³⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽⁴⁾ .	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
4. The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 98: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.	250	MHz

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 103: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 104: GTH Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTHRX}	Serial data rate		0.500	–	F _{GTHMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	

Table 110: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTYDRPCLK}	GTYDRPCLK maximum frequency.	250	MHz

Table 111: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range.		60	–	820	MHz
T _{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask⁽¹⁾

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL _{REFCLKMASK}	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
CPLL _{REFCLKMASK}	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 115: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Configuration Switching Characteristics

Table 127: Configuration Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T _{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T _{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
T _{PS_PROG_B}	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F _{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F _{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
F _{CFGMCLK}	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
F _{CFGMCLKTOL}	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T _{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1. XCZU2CG and XCZU2EG: -2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: -2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: -2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: -2E, -2I, -1E, -1I Added -2E ($V_{CCINT} = 0.85V$) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable. In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1. Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{REFPCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the <i>PS NAND Memory Controller Interface</i> section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU_REF_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the <i>PS-GTR Transceiver</i> section. Revised Table 70 and Table 71. Removed Note 8 from Table 74. Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90, and Table 91 to the Vivado Design Suite 2017.1 speed specifications. Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPPOUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPPOUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the <i>Integrated Interface Block for Interlaken</i> and <i>Integrated Interface Block for 100G Ethernet MAC and PCS</i> sections. Revised the <i>Configuration Switching Characteristics</i> section. Removed the <i>eFUSE Programming Conditions</i> table and added the specifications to Table 2 and Table 3.