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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 192K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu4cg-1sfvc784i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
V _{CCO_PSDDR}	PS DDR I/O supply voltage.	-0.500	1.650	V
V _{CC_PSDDR_PLL}	PS DDR PLL supply voltage.	-0.500	2.000	V
V _{CCO_PSIO}	PS I/O supply.	-0.500	3.630	V
V _{PSIN} ⁽²⁾	PS I/O input voltage.	-0.500	V _{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	-0.500	V _{CCO_PSDDR} + 0.550	V
V _{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	-0.500	2.000	V
Programmable Logic (PL)				
V _{CCINT}	Internal supply voltage.	-0.500	1.000	V
V _{CCINT_IO} ⁽³⁾	Internal supply voltage for the I/O banks.	-0.500	1.000	V
V _{CCAUX}	Auxiliary supply voltage.	-0.500	2.000	V
V _{CCBRAM}	Supply voltage for the block RAM memories.	-0.500	1.000	V
V _{CCO}	Output drivers supply voltage for HD I/O banks.	-0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	-0.500	2.000	V
V _{CCAUX_IO} ⁽⁴⁾	Auxiliary supply voltage for the I/O banks.	-0.500	2.000	V
V _{REF}	Input reference voltage.	-0.500	2.000	V
V _{IN} ⁽²⁾⁽⁵⁾⁽⁷⁾	I/O input voltage for HD I/O banks. ⁽⁶⁾	-0.550	V _{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	-0.550	V _{CCO} + 0.550	V
I _{DC}	Available output current at the pad.	-20	20	mA
I _{RMS}	Available RMS output current at the pad.	-20	20	mA
GTH or GTY Transceiver				
V _{MGTAVCC}	Analog supply voltage for transceiver circuits.	-0.500	1.000	V
V _{MGTAVTT}	Analog supply voltage for transceiver termination circuits.	-0.500	1.300	V
V _{MGTVCCAUX}	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	-0.500	1.900	V
V _{MGTREFCLK}	Transceiver reference clock absolute input voltage.	-0.500	1.300	V
V _{MGTAVTTRCAL}	Analog supply voltage for the resistor calibration circuit of the transceiver column.	-0.500	1.300	V
V _{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	-0.500	1.200	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating. ⁽⁸⁾	-	10	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT} .	-	10	mA
I _{DCIN-GND}	DC input current for receiver input pins DC coupled RX termination = GND. ⁽⁹⁾	-	0	mA
I _{DCIN-PROG}	DC input current for receiver input pins DC coupled RX termination = programmable. ⁽¹⁰⁾	-	0	mA
I _{DCOUT-FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating.	-	6	mA
I _{DCOUT-MGTAVTT}	DC output current for transmitter pins DC coupled RX termination = V _{MGTAVTT} .	-	6	mA

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
PL System Monitor					
V _{CCADC}	PL System Monitor supply relative to GNDADC.	1.746	1.800	1.854	V
V _{REFP}	PL System Monitor externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T _j ⁽¹³⁾	Junction temperature operating range for extended (E) temperature devices. ⁽¹⁴⁾	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.	–40	–	125	°C

Notes:

- All voltages are relative to GND.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* ([UG583](#)).
- V_{CC_PSINTFP_DDR} must be tied to V_{CC_PSINTFP}.
- Includes V_{CCO_PSDDR} of 1.2V, 1.35V, 1.5V at ±5% and 1.1V +0.07V/–0.04V depending upon the tolerances required by specific memory standards.
- Applies to all PS I/O supply banks. Includes V_{CCO_PSIO} of 1.8V, 2.5V, and 3.3V at ±5%.
- If the battery-backed RAM or RTC is not used, connect V_{CC_PSBATT} to GND or V_{CC_PSAUX}. The V_{CC_PSAUX} maximum of 1.89V is acceptable on an unused V_{CC_PSBATT}.
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)). The SYSMON temperature measurement errors (that are described in [Table 69](#) and [Table 124](#)) must be accounted for in your design. For example, when using the PL system monitor with an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
- Devices labeled with the speed/temperature grade of -2LE normally operate under Extended (E) temperature grade specifications with a maximum junction temperature of 100°C. However, E temperature grade devices can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do at 100°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V _{CCO} + 0.30	100%	–0.30	100%
V _{CCO} + 0.35	100%	–0.35	90%
V _{CCO} + 0.40	100%	–0.40	78%
V _{CCO} + 0.45	100%	–0.45	40%
V _{CCO} + 0.50	100%	–0.50	24%
V _{CCO} + 0.55	100%	–0.55	18.0%
V _{CCO} + 0.60	100%	–0.60	13.0%
V _{CCO} + 0.65	100%	–0.65	10.8%
V _{CCO} + 0.70	92%	–0.70	9.0%
V _{CCO} + 0.75	92%	–0.75	7.0%
V _{CCO} + 0.80	92%	–0.80	6.0%
V _{CCO} + 0.85	92%	–0.85	5.0%
V _{CCO} + 0.90	92%	–0.90	4.0%
V _{CCO} + 0.95	92%	–0.95	2.5%

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 7: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V _{CCO} + 0.30	100%	–0.30	100%
V _{CCO} + 0.35	100%	–0.35	100%
V _{CCO} + 0.40	92%	–0.40	92%
V _{CCO} + 0.45	50%	–0.45	50%
V _{CCO} + 0.50	20%	–0.50	20%
V _{CCO} + 0.55	10%	–0.55	10%
V _{CCO} + 0.60	6%	–0.60	6%
V _{CCO} + 0.65	2%	–0.65	2%
V _{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μs.

Table 8: V_{PSIN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI at -40°C to 100°C	AC Voltage Undershoot	% of UI at -40°C to 100°C
$V_{CCO_PSIO} + 0.30$	100%	-0.30	100%
$V_{CCO_PSIO} + 0.35$	100%	-0.35	75%
$V_{CCO_PSIO} + 0.40$	100%	-0.40	45%
$V_{CCO_PSIO} + 0.45$	100%	-0.45	40%
$V_{CCO_PSIO} + 0.50$	75%	-0.50	10%
$V_{CCO_PSIO} + 0.55$	75%	-0.55	6%
$V_{CCO_PSIO} + 0.60$	60%	-0.60	2%
$V_{CCO_PSIO} + 0.65$	30%	-0.65	0%
$V_{CCO_PSIO} + 0.70$	20%	-0.70	0%
$V_{CCO_PSIO} + 0.75$	10%	-0.75	0%
$V_{CCO_PSIO} + 0.80$	10%	-0.80	0%
$V_{CCO_PSIO} + 0.85$	8%	-0.85	0%
$V_{CCO_PSIO} + 0.90$	6%	-0.90	0%
$V_{CCO_PSIO} + 0.95$	6%	-0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 23: LVDS_25 DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.	2.375	2.500	2.625	V
V_{IDIFF}	Differential input voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$	100	350	600 ⁽²⁾	mV
V_{ICM}	Input common-mode voltage.	0.300	1.200	1.425	V

Notes:

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no V_{CCO} requirements. Any V_{CCO} can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information.

Table 24: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}^{(1)}$	Supply voltage.		1.710	1.800	1.890	V
$V_{ODIFF}^{(2)}$	Differential output voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$	$R_T = 100\Omega$ across Q and \overline{Q} signals	247	350	454	mV
$V_{OCM}^{(2)}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and \overline{Q} signals	1.000	1.250	1.425	V
$V_{IDIFF}^{(3)}$	Differential input voltage: ($\overline{Q} - Q$), $\overline{Q} = \text{High}$ ($Q - \overline{Q}$), $Q = \text{High}$		100	350	600 ⁽³⁾	mV
$V_{ICM_DC}^{(4)}$	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
$V_{ICM_AC}^{(5)}$	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for $LVDS_PRE_EMPHASIS = \text{FALSE}$.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. $EQUALIZATION = \text{EQ_NONE}$ (Default).
5. External input common mode voltage specification for AC coupled configurations. $EQUALIZATION = \text{EQ_LEVEL0}$, EQ_LEVEL1 , EQ_LEVEL2 , EQ_LEVEL3 , EQ_LEVEL4 .

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 27 lists the production released Zynq UltraScale+ MPSoC, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Zynq UltraScale+ MPSoC Device Production Software and Speed Specification Release

Device	Speed Grade and V _{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCZU2CG	N/A	Vivado tools 2017.1 v1.10					
XCZU2EG	N/A	Vivado tools 2017.1 v1.10					
XCZU3CG	N/A	Vivado tools 2017.1 v1.10					
XCZU3EG	N/A	Vivado tools 2017.1 v1.10					
XCZU4CG	N/A						
XCZU4EG							
XCZU4EV							
XCZU5CG	N/A						
XCZU5EG							
XCZU5EV							
XCZU6CG	N/A	Vivado tools 2017.1 v1.10					
XCZU6EG		Vivado tools 2017.1 v1.10					
XCZU7CG	N/A						
XCZU7EG							
XCZU7EV							
XCZU9CG	N/A	Vivado tools 2017.1 v1.10					
XCZU9EG		Vivado tools 2017.1 v1.10					
XCZU11EG							
XCZU15EG							
XCZU17EG							
XCZU19EG							

Notes:

1. See Table 3 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Table 30: PS DDR Performance (Cont'd)

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR3	All FFV packages, FBVB900 and SFVC784	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SFVA625	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1333	664	1333	664	1333	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
DDR3L	All FFV packages, FBVB900 and SFVC784	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single rank component	664	1600	664	1600	664	1600	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1333	664	1333	664	1333	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR3	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁶⁾	664	1600	664	1600	664	1600	Mb/s
		Dual die package ⁽⁶⁾	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single die package ⁽⁶⁾	664	1333	664	1333	664	1333	Mb/s
		Dual die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁶⁾	664	1066	664	1066	664	1066	Mb/s

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
2. Includes: 1 rank 1 slot, dual-die package 2 rank.
3. Includes: 2 rank 1 slot.
4. Dual die package includes single die with ECC.
5. LPDDR4 support is only available as a 32-bit interface.
6. 64-bit LPDDR3 interface performance values are defined without ECC support.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	–	16.5	MHz
$T_{TTCICLKL}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	ns
$T_{TTCICLKH}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	–	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

Table 60: PS-GTR Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequencies supported.	PCI Express	100 MHz			
		SATA	125 MHz or 150 MHz			
		USB 3.0	26 MHz, 52 MHz, or 100 MHz			
		DisplayPort	27 MHz, 108 MHz, or 135 MHz			
		SGMII	125 MHz			
T _{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle.	Transceiver PLL only.	40	–	60	%
		USB 3.0 with reference clock <40 MHz.	47.5	–	52.5	%

Programmable Logic (PL) Switching Characteristics

Table 75 (high-density IOB (HD)) and Table 76 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF_DELAY_PAD_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF_DELAY_O_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF_DELAY_TD_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF_DELAY_TD_PAD}$ when the DCITERMDISABLE pin is used. In HD I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF_DELAY_TD_PAD}$ when the INTERMDISABLE pin is used.

IOB High Density (HD) Switching Characteristics

Table 75: IOB High Density (HD) Switching Characteristics

I/O Standards	$T_{INBUF_DELAY_PAD_I}$					$T_{OUTBUF_DELAY_O_PAD}$					$T_{OUTBUF_DELAY_TD_PAD}$					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_18_F	0.978	0.978	1.058	0.978	1.058	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
DIFF_HSTL_I_18_S	0.978	0.978	1.058	0.978	1.058	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns
DIFF_HSTL_I_F	0.978	0.978	1.058	0.978	1.058	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
DIFF_HSTL_I_S	0.978	0.978	1.058	0.978	1.058	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
DIFF_HSUL_12_F	0.911	0.911	0.977	0.911	0.977	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
DIFF_HSUL_12_S	0.911	0.911	0.977	0.911	0.977	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
DIFF_SSTL12_F	0.906	0.906	0.977	0.906	0.977	1.643	1.643	1.792	1.643	1.792	1.285	1.285	1.423	1.285	1.423	ns
DIFF_SSTL12_S	0.906	0.906	0.977	0.906	0.977	1.784	1.784	1.948	1.784	1.948	1.567	1.567	1.706	1.567	1.706	ns
DIFF_SSTL135_F	0.927	0.927	0.995	0.927	0.995	1.625	1.625	1.765	1.625	1.765	1.341	1.341	1.458	1.341	1.458	ns
DIFF_SSTL135_II_F	0.927	0.927	0.995	0.927	0.995	1.623	1.623	1.770	1.623	1.770	1.325	1.325	1.470	1.325	1.470	ns
DIFF_SSTL135_II_S	0.927	0.927	0.995	0.927	0.995	1.768	1.768	1.916	1.768	1.916	1.722	1.722	1.911	1.722	1.911	ns
DIFF_SSTL135_S	0.927	0.927	0.995	0.927	0.995	1.869	1.869	2.025	1.869	2.025	1.814	1.814	1.976	1.814	1.976	ns
DIFF_SSTL15_F	0.928	0.928	1.020	0.928	1.020	1.628	1.628	1.771	1.628	1.771	1.374	1.374	1.483	1.374	1.483	ns
DIFF_SSTL15_II_F	0.928	0.928	1.020	0.928	1.020	1.622	1.622	1.778	1.622	1.778	1.356	1.356	1.442	1.356	1.442	ns
DIFF_SSTL15_II_S	0.928	0.928	1.020	0.928	1.020	1.821	1.821	1.987	1.821	1.987	1.895	1.895	2.047	1.895	2.047	ns
DIFF_SSTL15_S	0.928	0.928	1.020	0.928	1.020	1.824	1.824	1.977	1.824	1.977	1.743	1.743	1.907	1.743	1.907	ns
DIFF_SSTL18_II_F	0.961	0.961	1.038	0.961	1.038	1.729	1.729	1.880	1.729	1.880	1.377	1.377	1.492	1.377	1.492	ns
DIFF_SSTL18_II_S	0.961	0.961	1.038	0.961	1.038	1.796	1.796	1.965	1.796	1.965	1.616	1.616	1.800	1.616	1.800	ns
DIFF_SSTL18_I_F	0.961	0.961	1.038	0.961	1.038	1.609	1.609	1.755	1.609	1.755	1.220	1.220	1.313	1.220	1.313	ns
DIFF_SSTL18_I_S	0.961	0.961	1.038	0.961	1.038	1.786	1.786	1.942	1.786	1.942	1.677	1.677	1.836	1.677	1.836	ns
HSTL_I_18_F	0.947	0.947	1.021	0.947	1.021	1.574	1.574	1.718	1.574	1.718	1.160	1.160	1.271	1.160	1.271	ns
HSTL_I_18_S	0.947	0.947	1.021	0.947	1.021	1.805	1.805	1.950	1.805	1.950	1.748	1.748	1.867	1.748	1.867	ns

Table 75: IOB High Density (HD) Switching Characteristics (Cont'd)

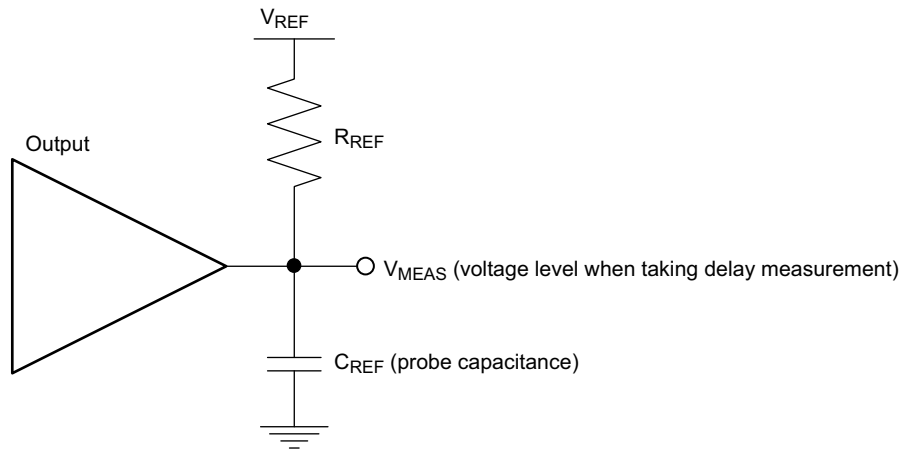
I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_F	0.856	0.856	0.900	0.856	0.900	1.611	1.611	1.762	1.611	1.762	1.313	1.313	1.417	1.313	1.417	ns
HSTL_I_S	0.856	0.856	0.900	0.856	0.900	1.798	1.798	1.913	1.798	1.913	1.630	1.630	1.780	1.630	1.780	ns
HSUL_12_F	0.780	0.780	0.867	0.780	0.867	1.573	1.573	1.703	1.573	1.703	1.222	1.222	1.335	1.222	1.335	ns
HSUL_12_S	0.780	0.780	0.867	0.780	0.867	1.711	1.711	1.864	1.711	1.864	1.536	1.536	1.665	1.536	1.665	ns
LVC MOS12_F_12	0.918	0.918	0.976	0.918	0.976	1.689	1.689	1.856	1.689	1.856	1.202	1.202	1.317	1.202	1.317	ns
LVC MOS12_F_4	0.918	0.918	0.976	0.918	0.976	1.742	1.742	1.922	1.742	1.922	1.353	1.353	1.478	1.353	1.478	ns
LVC MOS12_F_8	0.918	0.918	0.976	0.918	0.976	1.714	1.714	1.879	1.714	1.879	1.292	1.292	1.432	1.292	1.432	ns
LVC MOS12_S_12	0.918	0.918	0.976	0.918	0.976	2.073	2.073	2.247	2.073	2.247	1.581	1.581	1.717	1.581	1.717	ns
LVC MOS12_S_4	0.918	0.918	0.976	0.918	0.976	1.979	1.979	2.182	1.979	2.182	1.633	1.633	1.772	1.633	1.772	ns
LVC MOS12_S_8	0.918	0.918	0.976	0.918	0.976	2.205	2.205	2.406	2.205	2.406	1.767	1.767	1.928	1.767	1.928	ns
LVC MOS15_F_12	0.905	0.905	0.958	0.905	0.958	1.713	1.713	1.892	1.713	1.892	1.275	1.275	1.428	1.275	1.428	ns
LVC MOS15_F_16	0.905	0.905	0.958	0.905	0.958	1.722	1.722	1.881	1.722	1.881	1.260	1.260	1.407	1.260	1.407	ns
LVC MOS15_F_4	0.905	0.905	0.958	0.905	0.958	1.825	1.825	1.959	1.825	1.959	1.453	1.453	1.557	1.453	1.557	ns
LVC MOS15_F_8	0.905	0.905	0.958	0.905	0.958	1.778	1.778	1.930	1.778	1.930	1.378	1.378	1.458	1.378	1.458	ns
LVC MOS15_S_12	0.905	0.905	0.958	0.905	0.958	1.991	1.991	2.139	1.991	2.139	1.516	1.516	1.648	1.516	1.648	ns
LVC MOS15_S_16	0.905	0.905	0.958	0.905	0.958	2.172	2.172	2.389	2.172	2.389	1.707	1.707	1.888	1.707	1.888	ns
LVC MOS15_S_4	0.905	0.905	0.958	0.905	0.958	2.313	2.313	2.483	2.313	2.483	1.952	1.952	2.123	1.952	2.123	ns
LVC MOS15_S_8	0.905	0.905	0.958	0.905	0.958	2.170	2.170	2.400	2.170	2.400	1.817	1.817	1.984	1.817	1.984	ns
LVC MOS18_F_12	0.915	0.915	0.958	0.915	0.958	1.805	1.805	1.962	1.805	1.962	1.383	1.383	1.471	1.383	1.471	ns
LVC MOS18_F_16	0.915	0.915	0.958	0.915	0.958	1.785	1.785	1.917	1.785	1.917	1.338	1.338	1.446	1.338	1.446	ns
LVC MOS18_F_4	0.915	0.915	0.958	0.915	0.958	1.868	1.868	2.013	1.868	2.013	1.472	1.472	1.599	1.472	1.599	ns
LVC MOS18_F_8	0.915	0.915	0.958	0.915	0.958	1.797	1.797	1.979	1.797	1.979	1.384	1.384	1.487	1.384	1.487	ns
LVC MOS18_S_12	0.915	0.915	0.958	0.915	0.958	2.201	2.201	2.408	2.201	2.408	1.762	1.762	1.894	1.762	1.894	ns
LVC MOS18_S_16	0.915	0.915	0.958	0.915	0.958	2.173	2.173	2.362	2.173	2.362	1.702	1.702	1.834	1.702	1.834	ns
LVC MOS18_S_4	0.915	0.915	0.958	0.915	0.958	2.346	2.346	2.567	2.346	2.567	1.951	1.951	2.092	1.951	2.092	ns
LVC MOS18_S_8	0.915	0.915	0.958	0.915	0.958	2.292	2.292	2.511	2.292	2.511	1.848	1.848	2.008	1.848	2.008	ns
LVC MOS25_F_12	0.988	0.988	1.042	0.988	1.042	2.153	2.153	2.453	2.153	2.453	1.692	1.692	1.856	1.692	1.856	ns
LVC MOS25_F_16	0.988	0.988	1.042	0.988	1.042	2.105	2.105	2.406	2.105	2.406	1.623	1.623	1.786	1.623	1.786	ns
LVC MOS25_F_4	0.988	0.988	1.042	0.988	1.042	2.344	2.344	2.554	2.344	2.554	1.842	1.842	2.039	1.842	2.039	ns
LVC MOS25_F_8	0.988	0.988	1.042	0.988	1.042	2.184	2.184	2.516	2.184	2.516	1.726	1.726	1.910	1.726	1.910	ns
LVC MOS25_S_12	0.988	0.988	1.042	0.988	1.042	2.558	2.558	2.840	2.558	2.840	1.971	1.971	2.194	1.971	2.194	ns
LVC MOS25_S_16	0.988	0.988	1.042	0.988	1.042	2.449	2.449	2.740	2.449	2.740	1.852	1.852	2.063	1.852	2.063	ns
LVC MOS25_S_4	0.988	0.988	1.042	0.988	1.042	2.770	2.770	3.066	2.770	3.066	2.224	2.224	2.458	2.224	2.458	ns
LVC MOS25_S_8	0.988	0.988	1.042	0.988	1.042	2.663	2.663	2.963	2.663	2.963	2.091	2.091	2.373	2.091	2.373	ns
LVC MOS33_F_12	1.154	1.154	1.213	1.154	1.213	2.415	2.415	2.651	2.415	2.651	1.754	1.754	1.915	1.754	1.915	ns
LVC MOS33_F_16	1.154	1.154	1.213	1.154	1.213	2.383	2.383	2.603	2.383	2.603	1.734	1.734	1.869	1.734	1.869	ns
LVC MOS33_F_4	1.154	1.154	1.213	1.154	1.213	2.541	2.541	2.765	2.541	2.765	1.932	1.932	2.135	1.932	2.135	ns
LVC MOS33_F_8	1.154	1.154	1.213	1.154	1.213	2.603	2.603	2.822	2.603	2.822	1.937	1.937	2.130	1.937	2.130	ns
LVC MOS33_S_12	1.154	1.154	1.213	1.154	1.213	2.705	2.705	3.047	2.705	3.047	2.049	2.049	2.318	2.049	2.318	ns
LVC MOS33_S_16	1.154	1.154	1.213	1.154	1.213	2.714	2.714	3.024	2.714	3.024	2.028	2.028	2.232	2.028	2.232	ns
LVC MOS33_S_4	1.154	1.154	1.213	1.154	1.213	2.999	2.999	3.340	2.999	3.340	2.320	2.320	2.610	2.320	2.610	ns

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

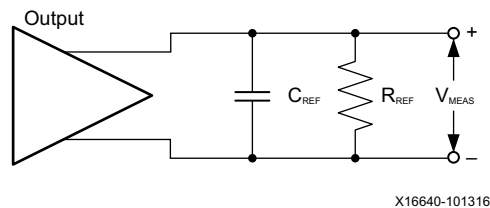
Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-101316

Figure 1: Single-Ended Test Setup



X16640-101316

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 79](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Table 92: Sampling Window

Description	Speed Grade and V _{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T _{SAMP_BUF} ⁽¹⁾	510	610	610	610	610	ps
T _{SAMP_NATIVE_DPA}	100	100	125	125	150	ps
T _{SAMP_NATIVE_BISC}	60	60	85	85	110	ps

Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

[Table 94](#) summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 94: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage.	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2}\right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽³⁾		–	100	–	nF

Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
- V_{RX_TERM} is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide (UG576)* for further information.

Table 97: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375 ⁽¹⁾		16.375 ⁽¹⁾				12.5				Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5				0.5				Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽²⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽³⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽⁴⁾ .	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLLRANGE}	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLLORANGE}	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1RANGE}	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 98: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.	250	MHz

Video Codec Performance

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoC EV devices that include the Video Codec unit (VCU).

Table 123: VCU Performance

Description	Speed Grade and V_{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
Video Codec decoder block maximum frequency (H.264/5 10-bit 4:2:2)	667	667	667	667	667	MHz

PL System Monitor Specifications

Table 124: PL SYSMON Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{CCADC} = 1.8V \pm 3\%$, $V_{REFP} = 1.25V$, $V_{REFN} = 0V$, $ADCCLK = 5.2\text{ MHz}$, $T_j = -40^\circ\text{C}$ to 100°C , typical values at $T_j = 40^\circ\text{C}$						
ADC Accuracy⁽¹⁾						
Resolution			10	–	–	Bits
Integral nonlinearity ⁽²⁾	INL		–	–	± 1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	± 1	LSBs
Offset error		Offset calibration enabled	–	–	± 2	LSBs
Gain error			–	–	± 0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		$T_j = -55^\circ\text{C}$ to 125°C	10	–	–	Bits
Integral nonlinearity ⁽²⁾	INL	$T_j = -55^\circ\text{C}$ to 125°C	–	–	± 1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic ($T_j = -55^\circ\text{C}$ to 125°C)	–	–	± 1	
Analog Inputs⁽²⁾						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/20/2017	1.3	<p>Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1.</p> <p>XCZU2CG and XCZU2EG: -2E, -2I, -1E, -1I XCZU3CG and XCZU3EG: -2E, -2I, -1E, -1I XCZU6CG and XCZU6EG: -2E, -2I, -1E, -1I XCZU9CG and XCZU9EG: -2E, -2I, -1E, -1I</p> <p>Added -2E ($V_{CCINT} = 0.85V$) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable.</p> <p>In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1.</p> <p>Revised V_{ICM} in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed F_{FTMCLK}. Updated $T_{REFPSCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the <i>PS NAND Memory Controller Interface</i> section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU_REF_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the <i>PS-GTR Transceiver</i> section. Revised Table 70 and Table 71. Removed Note 8 from Table 74.</p> <p>Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90, and Table 91 to the Vivado Design Suite 2017.1 speed specifications.</p> <p>Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised D_{VPP_OUT} in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised D_{VPP_OUT} in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the <i>Integrated Interface Block for Interlaken</i> and <i>Integrated Interface Block for 100G Ethernet MAC and PCS</i> sections. Revised the <i>Configuration Switching Characteristics</i> section. Removed the <i>eFUSE Programming Conditions</i> table and added the specifications to Table 2 and Table 3.</p>

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