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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 192K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu4cg-2fbvb900i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
V _{CCO} ⁽⁸⁾	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V _{CCAUX_IO} ⁽⁹⁾	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V _{IN} ⁽¹⁰⁾	I/O input voltage.	–0.200	–	V _{CCO} + 0.200	V
I _{IN} ⁽¹¹⁾	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
V _{MGTAVCC} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
V _{MGTAVTT} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
V _{MGTVCCAUX} ⁽¹²⁾	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
V _{MGTAVTTRCAL} ⁽¹²⁾	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V _{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 4: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
Differential termination	Programmable differential termination (TERM_100) for HP I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA .
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- I_{CC_PSBATT} is measured when the battery-backed RAM (BBRAM) is enabled.
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
- If VRP resides at a different bank (DCI cascade), the range increases to $\pm 15\%$.
- VRP resistor tolerance is $(240\Omega \pm 1\%)$
- On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 5: PS MIO Pull-up and Pull-down Current

Symbol	Description	Min	Max	Units
I_{RPU}	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 3.3V$.	20	80	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 2.5V$.	20	80	μA
	Pad pull-up (when selected) at $V_{IN} = 0V$, $V_{CCO_PSMIO} = 1.8V$.	15	65	μA
I_{RPD}	Pad pull-down (when selected) at $V_{IN} = 3.3V$.	20	80	μA
	Pad pull-down (when selected) at $V_{IN} = 2.5V$.	20	80	μA
	Pad pull-down (when selected) at $V_{IN} = 1.8V$.	15	65	μA

Table 9: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (Cont'd)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current.	XCZU2	N/A	26	26	26	26	mA
		XCZU3	N/A	26	26	26	26	mA
		XCZU4	32	32	32	32	32	mA
		XCZU5	32	32	32	32	32	mA
		XCZU6	33	33	33	33	33	mA
		XCZU7	56	56	56	56	56	mA
		XCZU9	33	33	33	33	33	mA
		XCZU11	56	56	56	56	56	mA
		XCZU15	33	33	33	33	33	mA
		XCZU17	74	74	74	74	74	mA
		XCZU19	74	74	74	74	74	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current.	XCZU2	N/A	6	6	6	6	mA
		XCZU3	N/A	6	6	6	6	mA
		XCZU4	9	9	9	9	9	mA
		XCZU5	9	9	9	9	9	mA
		XCZU6	25	24	24	24	24	mA
		XCZU7	16	15	15	15	15	mA
		XCZU9	25	24	24	24	24	mA
		XCZU11	23	22	22	22	22	mA
		XCZU15	29	28	28	28	28	mA
		XCZU17	37	35	35	35	35	mA
		XCZU19	37	35	35	35	35	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTAVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V_{ICM} (V) ⁽²⁾			V_{ID} (V) ⁽³⁾		V_{OL} (V) ⁽⁴⁾	V_{OH} (V) ⁽⁵⁾	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: Table 21 Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

Table 26: Speed Grade Designations by Device (Cont'd)

Device	Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU5EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU5EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU6CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU6EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU7CG	-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EG	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU7EV	-3E (V _{CCINT} = 0.90V), -2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V), -1LI (V _{CCINT} = 0.72V)		
XCZU9CG	-2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCZU9EG	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) -1LI (V _{CCINT} = 0.85V) -1LI (V _{CCINT} = 0.72V)		-2E (V _{CCINT} = 0.85V) -2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)

PS Configuration

Table 39: Processor Configuration Access Port Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: Boundary-Scan Port Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS eMMC Standard Interface

Table 46: eMMC Standard Interface⁽¹⁾

Symbol	Description	Min	Max	Units
eMMC Standard Interface				
T _{DCEMMCHSCLK}	eMMC clock duty cycle.	45	55	%
T _{EMMCHSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T _{EMMCHSDCK}	Input setup time, all inputs.	2.0	–	ns
T _{EMMCHSCKD}	Input hold time, all inputs.	2.0	–	ns
F _{EMMCHSCLK}	eMMC clock frequency.	–	25	MHz
eMMC High-Speed SDR Interface				
T _{DCEMMCHSCLK}	eMMC high-speed SDR clock duty cycle.	45	55	%
T _{EMMCHSCKO}	Clock to output delay, all outputs. ⁽²⁾	3.2	16.8	ns
T _{EMMCHSDIVW}	Input valid data window. ⁽³⁾	0.4	–	UI
F _{EMMCHSCLK}	eMMC high speed SDR clock frequency.	–	50	MHz
eMMC High-Speed DDR Interface				
T _{DCEMMCDDRCLK}	eMMC high-speed DDR clock duty cycle.	45	55	%
T _{EMMCDDRCKO1}	Data clock to output delay. ⁽²⁾	2.7	7.3	ns
T _{EMMCSDR1VW}	Input valid data window. ⁽³⁾	3.5	–	ns
T _{EMMCDDRCKO2}	Command clock to output delay.	3.2	16	ns
T _{EMMCDDRCK2}	Command input setup time.	3.9	–	ns
T _{EMMCDDRCKD2}	Command input hold time.	2.5	–	ns
F _{EMMCDDRCLK}	eMMC high-speed DDR clock frequency.	–	50	MHz
eMMC HS200 Interface				
T _{DCEMMCHS200CLK}	eMMC HS200 clock duty cycle.	40	60	%
T _{EMMCHS200CKO}	Clock to output delay, all outputs. ⁽²⁾	1.0	3.4	ns
T _{EMMCSDR1VW}	Input valid data window. ⁽³⁾	0.4	–	UI
F _{EMMCHS200CLK}	eMMC HS200 clock frequency.	–	200	MHz

Notes:

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	—	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	—	16.5	MHz
$T_{TTCICLKHL}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$T_{TTCICLKHL}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	—	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	—	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	—	100	MHz

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3 (1)	-2 (1)	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVC MOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVC MOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVC MOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVC MOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVC MOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVC MOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVC MOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVC MOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVC MOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVC MOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVC MOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVC MOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVC MOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVC MOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVC MOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVC MOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVC MOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVC MOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVC MOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVC MOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVC MOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVC MOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVC MOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVC MOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVC MOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVC MOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVC MOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVC MOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVC MOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVC MOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVC MOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

PLL Switching Characteristics

Table 86: PLL Specification⁽¹⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PLL_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	70	70	70	70	70	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
PLL_F _{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	750	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	1500	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3					
PLL_T _{OUTDUTY}	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100					μs
PLL_F _{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	667	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	2133	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. ⁽⁵⁾	5.86	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500, 1 x VCO mode: 750 0.5 x VCO mode: 375					MHz
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	667.5	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	70	MHz
PLL_F _{BANDWIDTH}	PLL bandwidth at typical.	14	14	14	14	14	MHz
PLL_F _{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTH transceivers.

GTH Transceiver DC Input and Output Levels

[Table 94](#) summarizes the DC specifications of the GTH transceivers in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 94: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage.	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based).	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (all packages).		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 103: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at the maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 104: GTH Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTHRX}	Serial data rate		0.500	–	F _{GTHMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 109: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F _{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYCRANGE}	CPLL line rate range ⁽¹⁾	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE1}	QPLL0 line rate range ⁽²⁾	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTYQRANGE2}	QPLL1 line rate range ⁽³⁾	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL0_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(2 \times \text{QPLL1_Frequency}) / \text{Output_Divider}$.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 117](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽²⁾	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽³⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽³⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale+ Integrated 100G Ethernet MAC/PCS](#). The *UltraScale Architecture and Product Overview (DS890)* lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 121: Maximum Performance for 100G Ethernet Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2 ⁽¹⁾	-1	-2	-1 ⁽²⁾	
F _{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V_{CCINT}=0.72V.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#). The *UltraScale Architecture and Product Overview (DS890)* lists the Zynq UltraScale+ MPSoCs that include this block.

Table 122: Maximum Performance for PCI Express Designs⁽¹⁾⁽²⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{CORECLK}	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
F _{MCAPCLK}	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Table 124: PL SYSMON Specifications (Cont'd)

Parameter	Symbol	Comments / Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error ⁽¹⁾⁽³⁾		$T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 3	$^{\circ}\text{C}$
		$T_j = -55^{\circ}\text{C}$ to 110°C (with internal REF)	–	–	± 3.5	$^{\circ}\text{C}$
		$T_j = 110^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 5	$^{\circ}\text{C}$
Supply sensor error ⁽⁴⁾		Supply voltages 0.72V to 1.2V, $T_j = -40^{\circ}\text{C}$ to 100°C (with external REF)	–	–	± 0.5	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -40^{\circ}\text{C}$ to 100°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -55^{\circ}\text{C}$ to 125°C (with external REF)	–	–	± 2.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -40^{\circ}\text{C}$ to 100°C (with internal REF)	–	–	± 1.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 2.0	%
		All other supply voltages, $T_j = -40^{\circ}\text{C}$ to 100°C (with internal REF)	–	–	± 1.5	%
		All other supply voltages, $T_j = -55^{\circ}\text{C}$ to 125°C (with internal REF)	–	–	± 2.5	%
Conversion Rate⁽⁵⁾						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference⁽⁶⁾						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $T_j = -55^{\circ}\text{C}$ to 125°C	1.225	1.25	1.275	V

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- When reading temperature values directly from the PMBus interface, the SYSMON has a $+4^{\circ}\text{C}$ offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of $\pm 3^{\circ}\text{C}$ becomes $+1^{\circ}\text{C}$ to $+7^{\circ}\text{C}$ when the temperature is read through the PMBus interface.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
- See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- Any variation in the reference voltage from the nominal $V_{\text{REFP}} = 1.25\text{V}$ and $V_{\text{REFN}} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

PL SYSMON I2C/PMBus Interfaces

Table 125: PL SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 126: PL SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.