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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 192K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BFBGA, FCBGA
Supplier Device Package	784-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu4cg-2sfvc784i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Video Codec Unit				
V _{CCINT_VCU}	Internal supply voltage for the video codec unit.	-0.500	1.000	V
PL System Monitor				
V _{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V _{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T _{STG}	Storage temperature (ambient).	-65	150	°C
T _{SOL}	Maximum soldering temperature. ⁽¹²⁾	-	260	°C
T _j	Maximum junction temperature. ⁽¹²⁾	-	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to [Table 6](#), [Table 7](#), and [Table 8](#) for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
7. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
12. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* ([UG1075](#)).

PS Configuration

Table 39: Processor Configuration Access Port Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: Boundary-Scan Port Switching Characteristics

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

- The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS Interface Specifications

PS Quad-SPI Controller Interface

Table 41: Generic Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 150 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK1}	Quad-SPI clock duty cycle.	15 pF	45	55	%
T _{QSPISSSCLK1}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
T _{QSPISCLKSS1}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
T _{QSPICKO1}	Clock to output delay, all outputs.	15 pF	2.9	4.5	ns
T _{QSPIDCK1}	Setup time, all inputs.	15 pF	0.9	–	ns
T _{QSPICKD1}	Hold time, all inputs.	15 pF	1.0	–	ns
F _{QSPICLK1}	Quad-SPI device clock frequency.	15 pF	–	150	MHz
F _{QSPIREFCLK1}	Quad-SPI reference clock frequency.	15 pF	–	300	MHz
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK2}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSSCLK2}	Slave select asserted to next clock edge.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS2}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO2}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK2}	Setup time, all inputs.	15 pF	2.3	–	ns
		30 pF	2.3	–	ns
T _{QSPICKD2}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPICLK2}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz
F _{QSPIREFCLK2}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz

Notes:

1. The test conditions are configured for the generic Quad-SPI interface at 150/100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for dual-parallel stacked or stacked modes.

Table 45: SD/SDIO Interface⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
F _{SDSDRCLK2}	SDR50 mode device clock frequency.	–	100	MHz
	SDR25 mode device clock frequency.	–	50	MHz
SD/SDIO Interface SDR12				
T _{DCSDHCLK3}	SD device clock duty cycle.	40	60	%
T _{SDSDRCKO3}	Clock to output delay, all outputs.	1.0	36.8	ns
T _{SDSDRDCK3}	Input setup time, all inputs.	24.0	–	ns
T _{SDSDRCKD3}	Input hold time, all inputs.	1.5	–	ns
F _{SDSDRCLK3}	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
T _{DCSDHCLK}	SD device clock duty cycle.	47	53	%
T _{SDHCKO}	Clock to output delay, all outputs. ⁽²⁾	2.2	13.8	ns
T _{SDHSDIVW}	Input valid data window. ⁽³⁾	0.35	–	UI
F _{SDHCLK}	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
T _{DCSDCLK}	SD device clock duty cycle.	45	55	%
T _{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T _{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T _{SDSCKD}	Input hold time, all inputs.	2.0	–	ns
F _{SDIDCLK}	Clock frequency in identification mode.	–	400	KHz
F _{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:

1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS Triple-timer Counter Interface

Table 54: Triple-timer Counter Interface

Symbol	Description	Min	Max	Units
$T_{PWTTCOCLK}$	Triple-timer counter output clock pulse width.	60.4	–	ns
$F_{TTCOCLK}$	Triple-timer counter output clock frequency.	–	16.5	MHz
$T_{TTCICLKHL}$	Triple-timer counter input clock high pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	ns
$T_{TTCICLKHL}$	Triple-timer counter input clock low pulse width.	$1.5 \times 1/F_{LPD_LSBUS_CTRLMAX}$	–	ns
$F_{TTCICLK}$	Triple-timer counter input clock frequency.	–	$F_{LPD_LSBUS_CTRLMAX}/3$	MHz

Notes:

1. All timing values assume an ideal external input clock. Your actual timing budget must account for additional external clock jitter.

PS Watchdog Timer Interface

Table 55: Watchdog Timer Interface

Symbol	Description	Min	Max	Units
F_{WDTCLK}	Watchdog timer input clock frequency.	–	100	MHz

Table 61: PS-GTR Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
PLL _{REFCLKMASK}	PLL reference clock select phase noise mask at REFCLK frequency = 25 MHz.	100	–	–	–102	dBc/Hz
		1 KHz	–	–	–124	
		10 KHz	–	–	–132	
		100 KHz	–	–	–139	
		1 MHz	–	–	–152	
		10 MHz	–	–	–154	
	PLL reference clock select phase noise mask at REFCLK frequency = 50 MHz.	100	–	–	–96	dBc/Hz
		1 KHz	–	–	–118	
		10 KHz	–	–	–126	
		100 KHz	–	–	–133	
		1 MHz	–	–	–146	
	PLL reference clock select phase noise mask at REFCLK frequency = 100 MHz.	100	–	–	–90	dBc/Hz
		1 KHz	–	–	–112	
		10 KHz	–	–	–120	
		100 KHz	–	–	–127	
		1 MHz	–	–	–140	
	PLL reference clock select phase noise mask at REFCLK frequency = 125 MHz.	100	–	–	–88	dBc/Hz
		1 KHz	–	–	–110	
		10 KHz	–	–	–118	
		100 KHz	–	–	–125	
1 MHz		–	–	–138		
PLL reference clock select phase noise mask at REFCLK frequency = 150 MHz.	100	–	–	–86	dBc/Hz	
	1 KHz	–	–	–108		
	10 KHz	–	–	–116		
	100 KHz	–	–	–123		
	1 MHz	–	–	–136		
		10 MHz	–	–	–138	

Notes:

- For reference clock frequencies not in this table, use the phase noise mask for the nearest reference clock frequency.

Table 62: PS-GTR Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTRTX}	Serial data rate range.		1.25	–	6.0	Gb/s
T _{RTX}	TX rise time.	20%–80%	–	65	–	ps
T _{FTX}	TX fall time.	80%–20%	–	65	–	ps

Table 72: MIPI D-PHY Performance

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3 ⁽¹⁾	-2 ⁽¹⁾	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:

1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: LVDS Native-Mode 1000BASE-X Support⁽¹⁾

Description	I/O Bank Type	Speed Grade and V _{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* ([UG583](#)), electrical analysis, and characterization of the system.

Table 74: Maximum Physical Interface (PHY) Rate for Memory Interfaces

Memory Standard	Package ⁽¹⁾	DRAM Type	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾⁽⁴⁾	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM ⁽²⁾⁽³⁾	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM ⁽²⁾⁽⁵⁾	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM ⁽²⁾⁽⁶⁾	1066	1066	1066	1066	800	Mb/s

Table 76: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}					T _{OUTBUF_DELAY_O_PAD}					T _{OUTBUF_DELAY_TD_PAD}					Units
	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	0.90V		0.85V		0.72V	
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.399	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.399	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.399	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.399	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.400	0.408	0.408	0.428	0.408	0.428	0.530	0.530	0.556	0.530	0.556	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.400	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.400	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.337	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.337	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.337	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.620	0.660	0.660	0.692	0.660	0.692	969.863	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 77 specifies the values of T_{OUTBUF_DELAY_TE_PAD} and T_{INBUF_DELAY_IBUFDIS_O}. T_{OUTBUF_DELAY_TE_PAD} is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{INBUF_DELAY_IBUFDIS_O} is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the DCITERMDISABLE pin is used. In HD I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{OUTBUF_DELAY_TE_PAD} when the INTERMDISABLE pin is used.

Table 77: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V		0.85V		0.72V	
		-3	-2	-1	-2	-1	
T _{OUTBUF_DELAY_TE_PAD}	T input to pad high-impedance for HD I/O banks	6.318	6.318	6.369	6.318	6.369	ns
	T input to pad high-impedance for HP I/O banks	5.330	5.330	5.341	5.330	5.341	ns
T _{INBUF_DELAY_IBUFDIS_O}	IBUF turn-on time from IBUFDISABLE to O output for HD I/O banks	2.266	2.266	2.430	2.266	2.430	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	0.936	0.936	1.037	0.936	1.037	ns

Table 78: Input Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0 ⁽⁶⁾	–
SLVS, 2.5V	SLVS_400_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
LVPECL, 2.5V	LVPECL	1.25 – 0.125	1.25 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0 ⁽⁶⁾	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0 ⁽⁶⁾	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H .
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in [Figure 1](#).
6. The value given is the differential input voltage.

Table 79: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V _{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V _{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	50	0	V _{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	50	0	V _{REF}	0.75
SSTL18, class I and class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
POD10, 1.0V	POD10	50	0	V _{REF}	1.0
POD12, 1.2V	POD12	50	0	V _{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V _{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V _{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V _{REF}	0.6
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	50	0	V _{REF}	0.675
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	50	0	V _{REF}	0.75
DIFF_SSTL18, class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V _{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V _{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 ⁽²⁾	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 ⁽²⁾	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 ⁽²⁾	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 80: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F _{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T _{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

DSP48 Slice Switching Characteristics

Table 83: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	With all registers used.	891	775	645	644	600	MHz
F _{MAX_PATDET}	With pattern detector.	794	687	571	562	524	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	635	544	456	440	413	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	577	492	410	395	371	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG.	655	565	468	453	423	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	483	410	338	323	304	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	280	MHz

Clock Buffers and Networks

Table 84: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL)							
F _{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	667	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)							
F _{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	667	MHz
Global Clock Buffer with Clock Enable (BUFGCE)							
F _{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	667	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)							
F _{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	667	MHz
GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)							
F _{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	512	MHz

MMCM Switching Characteristics

Table 85: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	800	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max					
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75					%
	Input duty cycle range: 50–199 MHz.	30–70					%
	Input duty cycle range: 200–399 MHz.	35–65					%
	Input duty cycle range: 400–499 MHz.	40–60					%
	Input duty cycle range: >500 MHz.	45–55					%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3					
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	667	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max					
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	450	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle					

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI

Table 115: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 116: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)		–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance⁽²⁾						
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s	0.25	–	–	UI
J _{T_SJ28.21}	Sinusoidal jitter (QPLL) ⁽³⁾	28.21 Gb/s	0.30	–	–	UI
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI
J _{T_SJ8.0}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI
J _{T_SJ6.6}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 117](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 117: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽²⁾	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽³⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽³⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Table 119: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units	
		0.90V		0.85V			0.72V						
		-3 ⁽¹⁾		-2 ⁽¹⁾		-1	-2		-1				
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	440.79		440.79			N/A	402.84		N/A			MHz
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	440.79		440.79			N/A	402.84		N/A			MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00			N/A	250.00		N/A			MHz
		Min ⁽²⁾	Max	Min ⁽²⁾	Max	Min	Max	Min ⁽²⁾	Max	Min	Max		
F _{CORE_CLK}	Interlaken core clock	412.50 ⁽³⁾	479.20	412.50 ⁽³⁾	479.20	N/A		412.50	429.69	N/A		MHz	
F _{LBUS_CLK}	Interlaken local bus clock	300.00 ⁽⁴⁾	349.52	300.00 ⁽⁴⁾	349.52	N/A		300.00	349.52	N/A		MHz	

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages						Units
		0.90V		0.85V		0.72V		
		-3		-2	-1	-2	-1	
F _{RX_SERDES_CLK}	Receive serializer/deserializer clock	402.84		402.84	N/A	N/A	N/A	MHz
F _{TX_SERDES_CLK}	Transmit serializer/deserializer clock	402.84		402.84	N/A	N/A	N/A	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00	N/A	N/A	N/A	MHz
F _{CORE_CLK}	Interlaken core clock	412.50		412.50	N/A	N/A	N/A	MHz
F _{LBUS_CLK}	Interlaken local bus clock	349.52		349.52	N/A	N/A	N/A	MHz

Table 124: PL SYSMON Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensor Accuracy						
Temperature sensor error ⁽¹⁾⁽³⁾		$T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 3	$^\circ\text{C}$
		$T_j = -55^\circ\text{C}$ to 110°C (with internal REF)	–	–	± 3.5	$^\circ\text{C}$
		$T_j = 110^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 5	$^\circ\text{C}$
Supply sensor error ⁽⁴⁾		Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with external REF)	–	–	± 0.5	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with external REF)	–	–	± 1.0	%
		All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with external REF)	–	–	± 2.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF)	–	–	± 1.0	%
		Supply voltages 0.72V to 1.2V, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 2.0	%
		All other supply voltages, $T_j = -40^\circ\text{C}$ to 100°C (with internal REF)	–	–	± 1.5	%
		All other supply voltages, $T_j = -55^\circ\text{C}$ to 125°C (with internal REF)	–	–	± 2.5	%
Conversion Rate⁽⁵⁾						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference⁽⁶⁾						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $T_j = -40^\circ\text{C}$ to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, $T_j = -55^\circ\text{C}$ to 125°C	1.225	1.25	1.275	V

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- When reading temperature values directly from the PMBus interface, the SYSMON has a $+4^\circ\text{C}$ offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of $\pm 3^\circ\text{C}$ becomes $+1^\circ\text{C}$ to $+7^\circ\text{C}$ when the temperature is read through the PMBus interface.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
- See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)).
- Any variation in the reference voltage from the nominal $V_{\text{REFP}} = 1.25\text{V}$ and $V_{\text{REFN}} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted.

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