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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 192K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu4cg-l1fbvb900i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
V _{CCO} ⁽⁸⁾	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V _{CCAUX_IO} ⁽⁹⁾	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V _{IN} ⁽¹⁰⁾	I/O input voltage.	–0.200	–	V _{CCO} + 0.200	V
I _{IN} ⁽¹¹⁾	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
V _{MGTAVCC} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
V _{MGTAVTT} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
V _{MGTVCCAUX} ⁽¹²⁾	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
V _{MGTAVTTRCAL} ⁽¹²⁾	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V _{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

PL I/O Levels

Table 14: SelectIO DC Input and Output Levels For HD I/O Banks⁽¹⁾⁽²⁾⁽³⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LVTTL	-0.300	0.800	2.000	3.400	0.400	2.400	Note 5	Note 5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL135_II	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL15_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.0	-8.0
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4
MIPI_DPHY_DCI_LP ⁽⁶⁾	-0.300	0.550	0.880	$V_{CCO} + 0.300$	0.050	1.100	0.01	-0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
3. POD10 and POD12 DC input and output levels are shown in [Table 16](#), [Table 20](#), [Table 21](#), and [Table 22](#).
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

PS Switching Characteristics

PS Clocks

Table 34: PS Reference Clock Requirements⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
T_{RFPCLK}	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:

1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: PS RTC Crystal Requirements⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	K Ω
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:

1. Required board components: Feedback resistor = 4.7 M Ω , PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: PS PLL Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	μ s
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

PS SPI Controller Interface

Table 48: SPI Interfaces⁽¹⁾

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSCLK}$	Slave select asserted to first active clock edge.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1 ⁽²⁾	–	$F_{SPI_REF_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI_REF_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI_REF_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: CAN Interface⁽¹⁾

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	μs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	μs
$F_{CAN_REF_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS-GTR Transceiver

Table 56: PS-GTR Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.		75	–	V _{PS_MGTRAVCC}	mV
V _{CMIN}	Common mode input voltage.		–	0	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage. ⁽¹⁾	Transmitter output swing is set to maximum value.	800	–	–	mV
V _{CMOUTAC}	Common mode output voltage: AC coupled (equation based).		$V_{PS_MGTRAVCC} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance.		–	100	–	Ω
R _{OUT}	Differential output resistance.		–	100	–	Ω
R _{MGTRREF}	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–	20	ps
C _{EXT}	Recommended external AC coupling capacitor. ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: PS-GTR Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R _{IN}	Differential input resistance.	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 58: PS-GTR Transceiver Performance

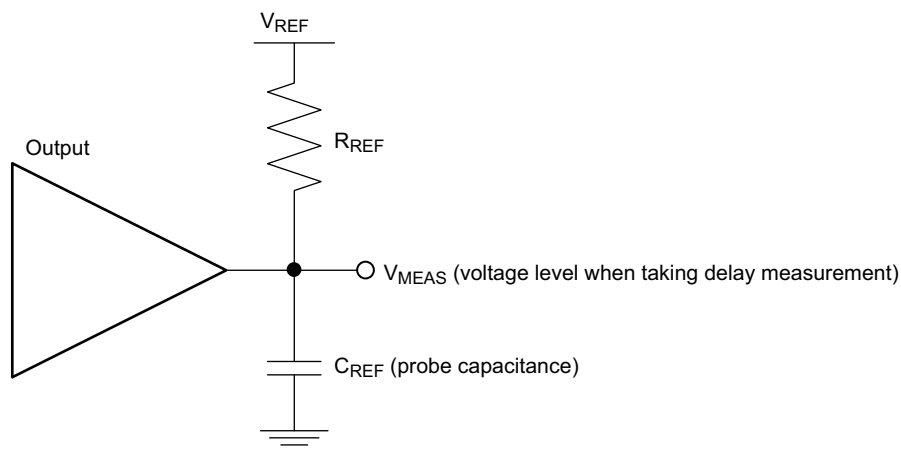
Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{GTRMAX}	PS-GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F _{GTRMIN}	PS-GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 59: PS-GTR Transceiver PLL/Lock Time Adaptation

Symbol	Description	Min	Typ	Max	Units
T _{LOCK}	Initial PLL lock.	–	–	0.11	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24 x 10 ⁶	UI

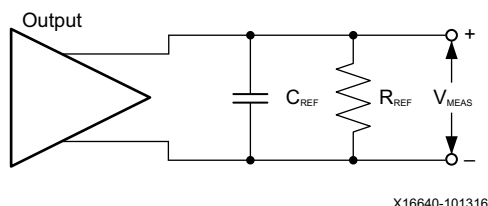
Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



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Figure 1: Single-Ended Test Setup



X16640-101316

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 79](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 85: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F _{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Table 88: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.								
T _{ICKOF_FAR}	Global clock input and output flip-flop <i>without</i> MMCM (far clock region).	XCZU2	N/A	5.27	5.68	5.80	6.13	ns
		XCZU3	N/A	5.27	5.68	5.80	6.13	ns
		XCZU4	5.07	6.06	6.61	6.23	7.10	ns
		XCZU5	5.07	6.06	6.61	6.23	7.10	ns
		XCZU6	5.38	6.49	6.97	7.14	7.59	ns
		XCZU7	5.39	6.54	7.01	7.16	7.62	ns
		XCZU9	5.38	6.49	6.97	7.14	7.59	ns
		XCZU11	6.18	7.41	8.11	7.66	8.99	ns
		XCZU15	5.38	6.49	6.96	7.19	7.71	ns
		XCZU17	6.21	7.53	8.07	8.36	8.90	ns
		XCZU19	6.21	7.53	8.07	8.36	8.90	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.

Table 89: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.								
T _{ICKOFMMCMCC}	Global clock input and output flip-flop <i>with</i> MMCM.	XCZU2	N/A	2.22	2.43	2.96	2.94	ns
		XCZU3	N/A	2.22	2.43	2.96	2.94	ns
		XCZU4	2.47	2.47	2.78	3.04	3.35	ns
		XCZU5	2.47	2.47	2.78	3.04	3.35	ns
		XCZU6	2.15	2.15	2.36	2.86	2.86	ns
		XCZU7	2.32	2.32	2.57	3.06	3.13	ns
		XCZU9	2.15	2.15	2.36	2.86	2.86	ns
		XCZU11	2.64	2.64	2.96	3.25	3.55	ns
		XCZU15	2.18	2.18	2.38	2.88	2.90	ns
		XCZU17	2.44	2.44	2.66	3.19	3.17	ns
XCZU19	2.44	2.44	2.66	3.19	3.17	ns		

Notes:

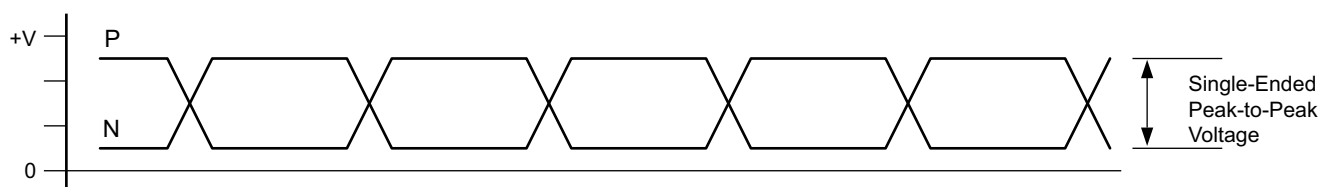
1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 92: Sampling Window

Description	Speed Grade and V _{CCINT} Operating Voltages					Units
	0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	
T _{SAMP_BUFG} ⁽¹⁾	510	610	610	610	610	ps
T _{SAMP_NATIVE_DPA}	100	100	125	125	150	ps
T _{SAMP_NATIVE_BISC}	60	60	85	85	110	ps

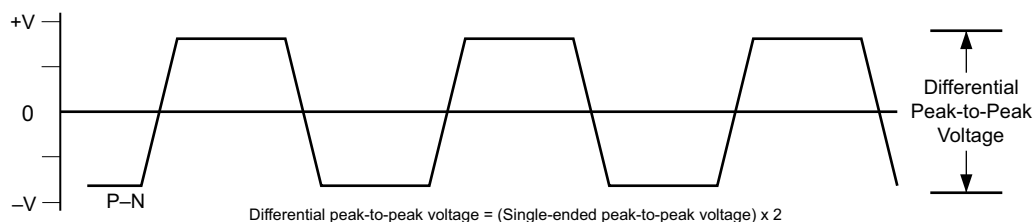
Notes:

1. This parameter indicates the total sampling error of the Zynq UltraScale+ MPSoC DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.



X16653-101316

Figure 3: Single-Ended Peak-to-Peak Voltage



X16639-101316

Figure 4: Differential Peak-to-Peak Voltage

Table 95 and Table 96 summarize the DC specifications of the GTH transceivers input and output clocks in Zynq UltraScale+ MPSoC. Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further details.

Table 95: GTH Transceiver Clock Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 96: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N.	$R_T = 100\Omega$ across P and N signals	100	–	330	mV
V_{OH}	Output High voltage for P and N.	$R_T = 100\Omega$ across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage. (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage.	$R_T = 100\Omega$ across P and N signals	300	–	500	mV

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 97: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade and V _{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F _{GTHMAX}	GTH maximum line rate.		16.375 ⁽¹⁾		16.375 ⁽¹⁾		12.5		12.5		10.3125		Gb/s
F _{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHCRANGE}	CPLL line rate range ⁽²⁾ .	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE1}	QPLL0 line rate range ⁽³⁾ .	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{GTHQRANGE2}	QPLL1 line rate range ⁽⁴⁾ .	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F _{CPLL} RANGE	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
F _{QPLL0} RANGE	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F _{QPLL1} RANGE	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:

1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation $(2 \times \text{CPLL_Frequency}) / \text{Output_Divider}$.
3. The values listed are the rounded results of the calculated equation $(\text{QPLL0_Frequency}) / \text{Output_Divider}$.
4. The values listed are the rounded results of the calculated equation $(\text{QPLL1_Frequency}) / \text{Output_Divider}$.

Table 98: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Speed Grades	Units
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency.	250	MHz

Table 102: GTH Transceiver User Clock Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPROGDIV}	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{RXOUTPROGDIV}	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F _{TXIN}	TXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{RXIN}	RXUSRCLK ⁽⁶⁾ maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F _{TXIN2}	TXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F _{RXIN2}	RXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

- Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)).

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoCs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

[Table 106](#) and [Table 107](#) summarize the DC specifications of the GTY transceivers in Zynq UltraScale+ MPSoCs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further details.

Table 106: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 11111	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 114: GTY Transceiver User Clock Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXIN2}	TXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz
F _{RXIN2}	RXUSRCLK2 ⁽⁶⁾ maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		64	64	511.719	440.781	402.832	402.832	195.313	MHz
		64	128	255.859	220.391	201.416	201.416	97.656	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	350.000	257.813	MHz
		40	80	204.688	204.688	156.250	175.000	128.906	MHz
		80	80	409.375	352.625	322.266	352.625	156.250	MHz
		80	160	204.688	176.313	161.133	176.313	78.125	MHz

Notes:

- Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
- For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
- For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
- For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
- When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI

Table 115: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 116: GTY Transceiver Receiver Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units	
F _{GTYRX}	Serial data rate		0.500	–	F _{GTYMAX}	Gb/s	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾		Modulated at 33 kHz	–5000	–	0	ppm
R _{XRL}	Run length (CID)			–	–	256	UI
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm	
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm	
		Bit rates > 8.0 Gb/s	–200	–	200	ppm	
SJ Jitter Tolerance ⁽²⁾							
J _{T_SJ32.75}	Sinusoidal jitter (QPLL) ⁽³⁾	32.75 Gb/s	0.25	–	–	UI	
J _{T_SJ28.21}	Sinusoidal jitter (QPLL) ⁽³⁾	28.21 Gb/s	0.30	–	–	UI	
J _{T_SJ16.375}	Sinusoidal jitter (QPLL) ⁽³⁾	16.375 Gb/s	0.30	–	–	UI	
J _{T_SJ15.0}	Sinusoidal jitter (QPLL) ⁽³⁾	15.0 Gb/s	0.30	–	–	UI	
J _{T_SJ14.1}	Sinusoidal jitter (QPLL) ⁽³⁾	14.1 Gb/s	0.30	–	–	UI	
J _{T_SJ13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.30	–	–	UI	
J _{T_SJ12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.30	–	–	UI	
J _{T_SJ11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ9.953_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	9.953 Gb/s	0.30	–	–	UI	
J _{T_SJ8.0}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI	
J _{T_SJ6.6}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI	
J _{T_SJ5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI	
J _{T_SJ4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI	
J _{T_SJ3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI	
J _{T_SJ2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.30	–	–	UI	
J _{T_SJ1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.30	–	–	UI	
J _{T_SJ500}	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s ⁽⁷⁾	0.30	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾							
J _{T_TJSE3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI	
J _{T_TJSE6.6}		6.6 Gb/s	0.70	–	–	UI	
J _{T_SJSE3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.10	–	–	UI	
J _{T_SJSE6.6}		6.6 Gb/s	0.10	–	–	UI	

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
- Composite jitter with RX equalizer enabled. DFE disabled.

PL SYSMON I2C/PMBus Interfaces

Table 125: PL SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 126: PL SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1 . Updated Table 2 , Table 4 , Table 6 , Table 7 , and Table 9 . Revised the Power Supply Sequencing section including Table 10 . Added PS and VCU ramp times to Table 11 . Revised V_{ODIFF} in Table 24 . Updated Table 25 . Added Note 1 to Table 26 . Table 30 replaces the previous three PS memory performance tables. Added values to Table 34 , Table 37 , and Table 38 . Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the PS NAND Memory Controller Interface section. Added and updated data in Table 40 . Added Note 3 to Table 41 . Added Note 3 to Table 42 . Added Note 1 to Table 45 . Updated Table 48 and removed Note 3 . Added data to Table 56 . Updated Table 60 . Added Table 61 . Updated Table 63 . Revised Table 69 . Added data to Table 70 . Added Note 2 to Table 71 . Updated Table 74 and added Note 4 . Updated V_L and V_H values in Table 78 . Added T_{MINPER_CLK} , revised F_{REFCLK} , and Note 1 to Table 82 . Added $MMCM_F_{DPRCLK_MAX}$ to Table 85 and $PLL_F_{DPRCLK_MAX}$ to Table 86 . Added data to Table 94 , Table 96 , Table 98 , Table 101 , and updated the note references in Table 102 . Updated Table 103 and added Note 8 . Updated Table 104 and added Note 7 . Added more protocols, Note 1 and Note 2 to Table 105 . Removed the GTH Transceiver Protocol Jitter Characteristics section because it is covered in Table 105 . Added Note 1 to Table 109 . Added data to Table 106 , Table 108 , Table 110 , Table 113 . Added Note 2 to Table 112 . Added note references in Table 114 . Updated Table 115 and added Note 8 . Updated Table 116 and added Note 7 . Added more protocols and Note 3 to Table 117 . Removed the GTy Transceiver Protocol Jitter Characteristics section because it is covered in Table 117 . Revised Table 124 . Added T_{POR} and updated F_{ICAPCK} in Table 127 . Updated the Automotive Applications Disclaimer .
06/20/2016	1.1	Updated the Summary description. In Table 1 , revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU} , I_{RPD} , and Note 4 to Table 2 and updated $V_{PS_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5 . Updated Note 5 in Table 4 . Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added $MIPI_DPHY_DCI$ to Table 14 , Table 15 , and Table 17 . Updated Table 23 , including removing the V_{CCO} specification and adding Note 1 . Added Note 1 to Table 24 . Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28 . Updated the -2 value in Table 29 . Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33 . Added VCO frequencies to Table 36 . Added the T_{PSPOR} minimum to Table 37 and updated Note 1 . Added Table 38 . Added value delineation over V_{CCINT} operating voltages in Table 39 . Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the PS NAND Memory Controller Interface section. Revised some units and Note 1 in Table 41 and Table 42 . Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43 . Added $F_{TSI_REF_CLK}$ to Table 44 and updated Note 1 . In Table 45 , revised $T_{DCSDHCLK1}$, $T_{DCSDHCLK2}$, and $T_{DCSDHCLK3}$ and Note 1 . In Table 46 , revised Note 1 . In Table 47 , revised Note 1 . Revised Table 48 , including Note 1 , and added Note 2 and Note 3 . In Table 49 , Table 50 , Table 51 , and Table 53 , revised Note 1 . Updated Table 71 . Replaced Table 74 . Updated Table 75 and Table 76 . Updated Table 78 and Table 79 . In Table 80 , added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95 . Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97 . Added Table 100 and Table 112 . Added Note 2 to Table 106 . Revised data in Table 109 . Revised Table 114 . Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121 . Moved Table 123 . Revised INL in Table 124 . Added notes to Table 125 and Table 126 . In the eFUSE and Programming Conditions table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.