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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 256K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu5cg-2fbvb900e

Table 1: **Absolute Maximum Ratings**[1] *(Cont'd)*

Symbol	Description	Min	Max	Units
V_{CCO_PSDDR}	PS DDR I/O supply voltage.	−0.500	1.650	V
$V_{CC\_PSDDR\_PLL}$	PS DDR PLL supply voltage.	−0.500	2.000	V
V_{CCO_PSIO}	PS I/O supply.	−0.500	3.630	V
V_{PSIN}[2]	PS I/O input voltage.	−0.500	V_{CCO_PSIO} + 0.550	V
	PS DDR I/O input voltage.	−0.500	V_{CCO_PSDDR} + 0.550	V
V_{CC_PSBATT}	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	−0.500	2.000	V
Programmable Logic (PL)				
V_{CCINT}	Internal supply voltage.	−0.500	1.000	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks.	−0.500	1.000	V
V_{CCAUX}	Auxiliary supply voltage.	−0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories.	−0.500	1.000	V
V_{CCO}	Output drivers supply voltage for HD I/O banks.	−0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	−0.500	2.000	V
V_{CCAUX_IO}[4]	Auxiliary supply voltage for the I/O banks.	−0.500	2.000	V
V_{REF}	Input reference voltage.	−0.500	2.000	V
V_{IN}[2][5][7]	I/O input voltage for HD I/O banks. [6]	−0.550	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks.	−0.550	V_{CCO} + 0.550	V
I_{DC}	Available output current at the pad.	−20	20	mA
I_{RMS}	Available RMS output current at the pad.	−20	20	mA
GTH or GTY Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	−0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	−0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	−0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	−0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	−0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	−0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating. [8]	−	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	−	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND. [9]	−	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable. [10]	−	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	−	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	−	6	mA

Table 1: **Absolute Maximum Ratings**[1] *(Cont'd)*

Symbol	Description	Min	Max	Units
Video Codec Unit				
V_{CCINT_VCU}	Internal supply voltage for the video codec unit.	−0.500	1.000	V
PL System Monitor				
V_{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	−65	150	°C
T_{SOL}	Maximum soldering temperature.[12]	–	260	°C
T_j	Maximum junction temperature.[12]	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
7. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
12. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 2: **Recommended Operating Conditions**[1][2] *(Cont'd)*

Symbol	Description	Min	Typ	Max	Units
V_{CCO}[8]	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}[9]	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}[10]	I/O input voltage.	−0.200	–	$V_{CCO} + 0.200$	V
I_{IN}[11]	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$[12]	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$[12]	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$[12]	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$[12]	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V_{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 4: **DC Characteristics Over Recommended Operating Conditions** *(Cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
I_{CC_PSBATT}[4][5]	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC enabled.	–	–	3650	nA
	Battery supply current at V_{CC_PSBATT} = 1.50V, RTC disabled.	–	–	650	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC enabled.	–	–	3150	nA
	Battery supply current at V_{CC_PSBATT} = 1.20V, RTC disabled.	–	–	150	nA
I_{PSFS}[6]	PS V_{CC_PSAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in HP I/O banks[8] (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–10%[7]	40	+10%[7]	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–10%[7]	48	+10%[7]	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–10%[7]	60	+10%[7]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%[7]	40	+10%[7]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%[7]	48	+10%[7]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%[7]	60	+10%[7]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%[7]	120	+10%[7]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%[7]	240	+10%[7]	Ω
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HD I/O banks (measured per JEDEC specification)					
R[9]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks**[1][2][3]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	5.8	−5.8
HSTL_I_12	−0.300	V_{REF} − 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	−4.1
HSTL_I_18	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	6.2	−6.2
HSUL_12	−0.300	V_{REF} − 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
LVCMOS12	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	Note 4	Note 4
LVCMOS15	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	Note 5	Note 5
LVCMOS18	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	Note 5	Note 5
LVDCI_15	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	7.0	−7.0
LVDCI_18	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	7.0	−7.0
SSTL12	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.150	$V_{CCO}/2$ + 0.150	8.0	−8.0
SSTL135	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.150	$V_{CCO}/2$ + 0.150	9.0	−9.0
SSTL15	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.175	$V_{CCO}/2$ + 0.175	10.0	−10.0
SSTL18_I	−0.300	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.470	$V_{CCO}/2$ + 0.470	7.0	−7.0
MIPI_DPHY_DCI_LP[6]	−0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	−0.01

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards**[1][2]

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	−0.300	V_{REF} − 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	−0.300	V_{REF} − 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 25.

Table 25: **Speed Specification Version By Device**

2017.1	Device
1.08	XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU11EG
1.10	XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XCZU6CG, XCZU6EG, XCZU7CG, XCZU7EG, XCZU7EV, XCZU9CG, XCZU9EG, XCZU15EG, XCZU17EG, XCZU19EG

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq UltraScale+ MPSoC.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 26 correlates the current status of the Zynq UltraScale+ MPSoC on a per speed grade basis. See Table 3 for operating voltages listed by speed grade.

Table 26: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU2CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU2EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU3EG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU4CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU4EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Table 26: **Speed Grade Designations by Device** *(Cont'd)*

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU11EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU17EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**[1]

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:
1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**[1]

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:
1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	µs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

Table 42: **Linear Quad-SPI Interface**[1]

Symbol	Description	Load Conditions[2]	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
$T_{DCQSPICLK5}$	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
$T_{QSPISSSCLK5}$	Slave select asserted to next clock edge.[3]	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPISCLKSS5}$	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
$T_{QSPICKO5}$	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
$T_{QSPIDCK5}$	Setup time, all inputs.	15 pF	2.4	–	ns
		30 pF	2.4	–	ns
$T_{QSPICKD5}$	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
$F_{QSPIREFCLK5}$	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
$F_{QSPICLK5}$	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz

Notes:
1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. $T_{QSPISSSCLK5}$ is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

Table 43: **ULPI Interface**[1]

Symbol	Description	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs.	4.5	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs.	0	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs.	2.0	8.86	ns
$F_{ULPICLK}$	ULPI reference clock frequency.	–	60	MHz

Notes:
1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 45: **SD/SDIO Interface**[1] *(Cont'd)*

Symbol	Description	Min	Max	Units
$F_{SDSDRCLK2}$	SDR50 mode device clock frequency.	–	100	MHz
	SDR25 mode device clock frequency.	–	50	MHz
SD/SDIO Interface SDR12				
$T_{DCSDHSCLK3}$	SD device clock duty cycle.	40	60	%
$T_{SDSDRCKO3}$	Clock to output delay, all outputs.	1.0	36.8	ns
$T_{SDSDRDCK3}$	Input setup time, all inputs.	24.0	–	ns
$T_{SDSDRCKD3}$	Input hold time, all inputs.	1.5	–	ns
$F_{SDSDRCLK3}$	SDR12 mode device clock frequency.	–	25	MHz
SD/SDIO Interface High-Speed Mode				
$T_{DCSDHSCLK}$	SD device clock duty cycle.	47	53	%
$T_{SDHSCKO}$	Clock to output delay, all outputs.[2]	2.2	13.8	ns
$T_{SDHSDIVW}$	Input valid data window.[3]	0.35	–	UI
$F_{SDHSCLK}$	High-speed mode SD device clock frequency.	–	50	MHz
SD/SDIO Interface Standard Mode				
$T_{DCSDSCLK}$	SD device clock duty cycle.	45	55	%
T_{SDSCKO}	Clock to output delay, all outputs.	–2.0	4.5	ns
T_{SDSDCK}	Input setup time, all inputs.	2.0	–	ns
T_{SDSCKD}	Input hold time, all inputs.	2.0	–	ns
$F_{SDIDCLK}$	Clock frequency in identification mode.	–	400	KHz
F_{SDSCLK}	Standard SD device clock frequency.	–	19	MHz

Notes:
1. The test conditions SD/SDIO standard mode (default speed mode) use an 8 mA drive strength, fast slew rate, and a 30 pF load. For SD/SDIO high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other SD/SDIO modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

PS-GTR Transceiver

Table 56: **PS-GTR Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled).		100	–	1200	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.		75	–	$V_{PS\_MGTRAVCC}$	mV
V_{CMIN}	Common mode input voltage.		–	0	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage. [1]	Transmitter output swing is set to maximum value.	800	–	–	mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based).		$V_{PS\_MGTRAVCC} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance.		–	100	–	Ω
R_{OUT}	Differential output resistance.		–	100	–	Ω
$R_{MGTRREF}$	Resistor value between calibration resistor pin to GND.		497.5	500	502.5	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (All packages).		–	–	20	ps
C_{EXT}	Recommended external AC coupling capacitor. [2]		–	100	–	nF

Notes:
1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 57: **PS-GTR Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage.	250	–	2000	mV
R_{IN}	Differential input resistance.	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor.	–	10	–	nF

Table 58: **PS-GTR Transceiver Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTRMAX}	PS-GTR maximum line rate.	6.0	6.0	6.0	Gb/s
F_{GTRMIN}	PS-GTR minimum line rate.	1.25	1.25	1.25	Gb/s

Table 59: **PS-GTR Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock.	–	–	0.11	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	–	–	24×10^6	UI

IOB High Performance (HP) Switching Characteristics

Table 76: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.402	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.339	0.570	0.570	0.603	0.570	0.603	0.653	0.653	0.692	0.653	0.692	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.339	0.782	0.782	0.834	0.782	0.834	0.816	0.816	0.871	0.816	0.871	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.402	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.402	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.402	0.755	0.755	0.806	0.755	0.806	0.842	0.842	0.907	0.842	0.907	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.339	0.555	0.555	0.586	0.555	0.586	0.643	0.643	0.684	0.643	0.684	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.339	0.762	0.762	0.818	0.762	0.818	0.836	0.836	0.900	0.836	0.900	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.417	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.644	0.644	0.684	0.644	0.684	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.417	0.767	0.767	0.823	0.767	0.823	0.848	0.848	0.912	0.848	0.912	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.417	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.417	0.555	0.555	0.586	0.555	0.586	0.640	0.640	0.677	0.640	0.677	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.818	0.767	0.818	0.811	0.811	0.866	0.811	0.866	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.653	0.653	0.694	0.653	0.694	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.737	0.737	0.787	0.737	0.787	0.822	0.822	0.885	0.822	0.885	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.402	0.552	0.552	0.583	0.552	0.583	0.641	0.641	0.679	0.641	0.679	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.402	0.752	0.752	0.800	0.752	0.800	0.813	0.813	0.868	0.813	0.868	ns
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.430	0.425	0.425	0.444	0.425	0.444	0.555	0.555	0.584	0.555	0.584	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.430	0.542	0.542	0.571	0.542	0.571	0.640	0.640	0.681	0.640	0.681	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.430	0.754	0.754	0.815	0.754	0.815	0.850	0.850	0.917	0.850	0.917	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.433	0.438	0.438	0.459	0.438	0.459	0.569	0.569	0.601	0.569	0.601	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.433	0.538	0.538	0.568	0.538	0.568	0.630	0.630	0.667	0.630	0.667	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.433	0.766	0.766	0.821	0.766	0.821	0.836	0.836	0.894	0.836	0.894	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.432	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.432	0.543	0.543	0.572	0.543	0.572	0.638	0.638	0.678	0.638	0.678	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.432	0.772	0.772	0.822	0.772	0.822	0.862	0.862	0.929	0.862	0.929	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.430	0.455	0.455	0.476	0.455	0.476	0.595	0.595	0.626	0.595	0.626	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.430	0.551	0.551	0.582	0.551	0.582	0.641	0.641	0.679	0.641	0.679	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.430	0.767	0.767	0.817	0.767	0.817	0.832	0.832	0.889	0.832	0.889	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.400	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.400	0.557	0.557	0.587	0.557	0.587	0.654	0.654	0.694	0.654	0.694	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.400	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.908	0.842	0.908	ns

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Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 90 and Table 91 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 90: **Global Clock Input Setup and Hold With 3.3V HD I/O without MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]								
T_{PSFD_ZU2}	Global clock input and input flip-flop (or latch) without MMCM.	XCZU2 (Setup)	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU2}		XCZU2 (Hold)		−0.36	−0.36	−0.14	−0.14	ns
T_{PSFD_ZU3}		XCZU3 (Setup)	N/A	2.27	2.37	2.55	2.64	ns
T_{PHFD_ZU3}		XCZU3 (Hold)		−0.36	−0.36	−0.14	−0.14	ns
T_{PSFD_ZU4}		XCZU4 (Setup)	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU4}		XCZU4 (Hold)	−0.28	−0.28	−0.28	−0.09	−0.09	ns
T_{PSFD_ZU5}		XCZU5 (Setup)	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU5}		XCZU5 (Hold)	−0.28	−0.28	−0.28	−0.09	−0.09	ns
T_{PSFD_ZU6}		XCZU6 (Setup)	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU6}		XCZU6 (Hold)	−0.05	−0.05	−0.05	0.27	0.42	ns
T_{PSFD_ZU7}		XCZU7 (Setup)	1.43	2.32	2.42	2.60	2.69	ns
T_{PHFD_ZU7}		XCZU7 (Hold)	−0.40	−0.40	−0.40	−0.21	−0.21	ns
T_{PSFD_ZU9}		XCZU9 (Setup)	0.96	1.79	1.86	1.93	2.02	ns
T_{PHFD_ZU9}		XCZU9 (Hold)	−0.05	−0.05	−0.05	0.27	0.42	ns
T_{PSFD_ZU11}		XCZU11 (Setup)	1.28	2.01	2.07	2.59	2.59	ns
T_{PHFD_ZU11}		XCZU11 (Hold)	−0.29	−0.29	−0.29	−0.09	0.19	ns
T_{PSFD_ZU15}		XCZU15 (Setup)	0.96	1.79	1.85	1.92	2.01	ns
T_{PHFD_ZU15}		XCZU15 (Hold)	−0.04	−0.04	−0.04	0.27	0.43	ns
T_{PSFD_ZU17}		XCZU17 (Setup)	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU17}		XCZU17 (Hold)	−0.38	−0.38	−0.38	−0.19	−0.19	ns
T_{PSFD_ZU19}		XCZU19 (Setup)	1.41	2.29	2.38	2.57	2.65	ns
T_{PHFD_ZU19}		XCZU19 (Hold)	−0.38	−0.38	−0.38	−0.19	−0.19	ns

Notes:
1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 102: **GTH Transceiver User Clock Switching Characteristics[1]** *(Cont'd)*

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V and 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 103: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500.00	ps
$T_{J16.375}$	Total jitter[2][4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J15.0}$	Total jitter[2][4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2][4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2][4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter[2][4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter[2][4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter[3][4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter[2][4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter[2][4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter[3][4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter[2][4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter[3][4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter[3][4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter[3][4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3][4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3][4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J4.0}$	Total jitter[3][4]	4.0 Gb/s	–	–	0.32	UI
$D_{J4.0}$	Deterministic jitter[3][4]		–	–	0.16	UI
$T_{J3.20}$	Total jitter[3][4]	3.20 Gb/s[5]	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter[3][4]		–	–	0.10	UI

Table 104: **GTH Transceiver Receiver Switching Characteristics** *(Cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s[7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:
1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 105. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 110: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
F$_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 111: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F$_{GCLK}$	Reference clock frequency range.		60	–	820	MHz
T$_{RCLK}$	Reference clock rise time.	20% – 80%	–	200	–	ps
T$_{FCLK}$	Reference clock fall time.	80% – 20%	–	200	–	ps
T$_{DCREF}$	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 112: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask[1]**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL$_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
CPLL$_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 113: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	**Typ**	**Max**	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 114: **GTY Transceiver User Clock Switching Characteristics**[1]

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	**Interconnect Logic**	**-3**[2]	**-2**[2][3]	**-1**[4][5]	**-2**[3]	**-1**[5]	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	322.266	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		64	64, 128	511.719	440.781	402.832	402.832	195.313	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	350.000	257.813	MHz
		80	80, 160	409.375	352.625	322.266	352.625	156.250	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale+ Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 121: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2[1]	-1	-2	-1[2]	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:
1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V_{CCINT}=0.72V.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include this block.

Table 122: **Maximum Performance for PCI Express Designs**[1][2]

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:
1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.