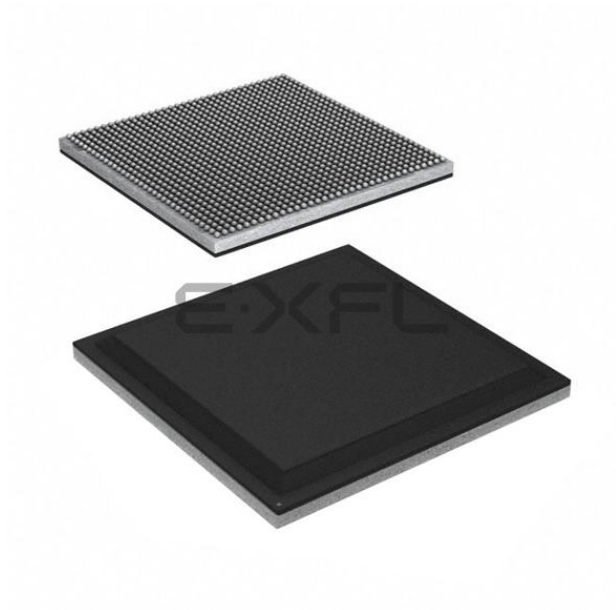
AMD Xilinx - XCZU6CG-1FFVB1156E Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 469K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu6cg-1ffvb1156e

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
V_{CCO}(8)	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(9)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(10)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(11)	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
$V_{MGTAVCC}$(12)	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(12)	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
$V_{MGTVCCAUX}$(12)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
$V_{MGTAVTTRCAL}$(12)	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V_{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Table 9: **Typical Quiescent Supply Current(1)(2)(3)(4) *(Cont'd)***

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current.	XCZU2	N/A	26	26	26	26	mA
		XCZU3	N/A	26	26	26	26	mA
		XCZU4	32	32	32	32	32	mA
		XCZU5	32	32	32	32	32	mA
		XCZU6	33	33	33	33	33	mA
		XCZU7	56	56	56	56	56	mA
		XCZU9	33	33	33	33	33	mA
		XCZU11	56	56	56	56	56	mA
		XCZU15	33	33	33	33	33	mA
		XCZU17	74	74	74	74	74	mA
		XCZU19	74	74	74	74	74	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XCZU2	N/A	6	6	6	6	mA
		XCZU3	N/A	6	6	6	6	mA
		XCZU4	9	9	9	9	9	mA
		XCZU5	9	9	9	9	9	mA
		XCZU6	25	24	24	24	24	mA
		XCZU7	16	15	15	15	15	mA
		XCZU9	25	24	24	24	24	mA
		XCZU11	23	22	22	22	22	mA
		XCZU15	29	28	28	28	28	mA
		XCZU17	37	35	35	35	35	mA
		XCZU19	37	35	35	35	35	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions or supplies other than those specified.
4. Typical values depend upon your configuration. To accurately estimate all PS supply currents, use the interactive XPE spreadsheet tool.

Table 15: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 16: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU5EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU5EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU6CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU6EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU7CG	-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU7EV	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU9CG	-2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCZU9EG	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V) -1LI (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.72V)		-2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)

Table 26: **Speed Grade Designations by Device *(Cont'd)***

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU11EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU17EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

Table 37: **PS Reset Assertion Timing Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time.(1)	10	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time.	3	–	–	PS_REF_CLK Clock Cycles

Notes:

1. PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: **PS Clocks Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{TOPSW\_MAINMAX}$	TOPSW_MAIN maximum frequency.	600	533	533	MHz
$F_{TOPSW\_LSBUSMAX}$	TOPSW_LSBUS maximum frequency.	100	100	100	MHz
$F_{GDMAMAX}$	FPD-DMA maximum frequency.	600	600	600	MHz
$F_{DPDMAMAX}$	DisplayPort DMA maximum frequency.	600	600	600	MHz
$F_{LPD\_SWITCH\_CTRLMAX}$	LPD_SWITCH_CTRL maximum frequency.	600	500	500	MHz
$F_{LPD\_LSBUS\_CTRLMAX}$	LPD_LSBUS_CTRL maximum frequency.	100	100	100	MHz
$F_{ADMAMAX}$	LPD-DMA maximum frequency.	600	500	500	MHz
$F_{APLL\_TO\_LPDMAX}$	APLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{DPLL\_TO\_LPDMAX}$	DPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{VPLL\_TO\_LPDMAX}$	VPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{IOPLL\_TO\_LPDMAX}$	IOPLL_TO_LPD maximum frequency.	533	533	533	MHz
$F_{RPLL\_TO\_FPDMAX}$	RPLL_TO_FPD maximum frequency.	533	533	533	MHz

PS SPI Controller Interface

Table 48: **SPI Interfaces**(1)

Symbol	Description	Min	Max	Units
SPI Master Interface				
$T_{DCMSPICLK}$	SPI master mode clock duty cycle.	45	55	%
$T_{MSPISSSCLK}$	Slave select asserted to first active clock edge.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted.	1(2)	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{MSPIDCK}$	Input setup time for MISO.	–2.0	–	ns
$T_{MSPICKD}$	Input hold time for MISO.	0.3	–	$F_{MSPICLK}$ cycles
$T_{MSPICKO}$	MOSI and slave select clock to out delay.	–2.0	5.0	ns
$F_{MSPICLK}$	SPI master device clock frequency.	–	50	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz
SPI Slave Interface				
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted.	2	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPIDCK}$	Input setup time for MOSI.	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MOSI.	1	–	$F_{SPI\_REF\_CLK}$ cycles
$T_{SSPICKO}$	MISO clock to out delay.	0.0	13.0	ns
$F_{SSPICLK}$	SPI slave mode device clock frequency.	–	25	MHz
$F_{SPI\_REF\_CLK}$	SPI reference clock frequency.	–	200	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 30 pF load.
2. Valid when two SPI_REF_CLK delays are programmed between CS and CLK for $T_{MSPISSSCLK}$, and between CLK and CS for $T_{MSPISCLKSS}$ in the SPI delay_reg0 register.

PS CAN Controller Interface

Table 49: **CAN Interface**(1)

Symbol	Description	Min	Max	Units
$T_{PWCANRX}$	Receive pulse width.	1.0	–	µs
$T_{PWCANTX}$	Transmit pulse width.	1.0	–	µs
$F_{CAN\_REF\_CLK}$	Internally sourced CAN reference clock frequency.	–	100	MHz
	Externally sourced CAN reference clock frequency.	–	40	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 72: **MIPI D-PHY Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3[1]	-2[1]	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Notes:
1. In the SBVA484 package, the data rate is 1260 Mb/s.

Table 73: **LVDS Native-Mode 1000BASE-X Support[1]**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:
1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 74 provides the maximum data rates for applicable memory standards using the Zynq UltraScale+ MPSoC memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	Package[1]	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages and FBVB900	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM[2][3][4]	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM[2][5]	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM[2][6]	1600	1600	1333	1333	N/A	Mb/s
	SFVC784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM[2][3]	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM[2][5]	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages and FBVB900	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM[2][3]	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM[2][5]	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM[2][6]	1066	1066	1066	1066	800	Mb/s
	SFVC784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM[2][3]	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM[2][5]	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM[2][6]	1066	1066	1066	1066	800	Mb/s

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces *(Cont'd)***

Memory Standard	Package(1)	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM(2)(3)	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM(2)(5)	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM(2)(6)	800	800	800	800	606	Mb/s
QDR II+	All	Single rank component(7)	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:

1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Table 76: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoC that include this memory.

Table 81: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F_{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	481	MHz
F_{MAX_ECC}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	315	MHz
$F_{MAX\_NORPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	408	MHz
T_{PW} (1)	Minimum pulse width.	650	700	730	800	832	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle					

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F_{REFCLK}	REFCLK frequency for IDELAYCTRL (component mode).	300 to 800					MHz
	REFCLK frequency for BITSLICE_CONTROL (native mode). (1)	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	300 to 2133	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock.	3.195	3.195	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width.	52.00					ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution.	2.1 to 12					ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

Table 85: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 102: **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 105: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(1)	IEEE 802.3-2012	10.3125	Compliant
40GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
TFI-5	OIF-TFI5-0.1.0	2.488	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(2)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(2)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys Bandwidth Engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI(2)	HDMI 2.0	All	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort(2)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	up to 11.180997	Compliant

Notes:
1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

Table 115: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Table 117: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale+ Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Zynq UltraScale+ MPSoC.

Table 121: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2(1)	-1	-2	-1(2)	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	250.00	MHz

Notes:
1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where V_{CCINT}=0.72V.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists the Zynq UltraScale+ MPSoCs that include this block.

Table 122: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	125.00	MHz

Notes:
1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Configuration Switching Characteristics

Table 127: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
PL Power-up Timing Characteristics							
T_{PL}	PS_PROG_B PL latency.	7.5	7.5	7.5	7.5	7.5	ms, Max
T_{POR}	Power-on reset from PL power-on to PL ready to configure (40 ms maximum ramp rate).	65	65	65	65	65	ms, Max
		0	0	0	0	0	ms, Min
	Power-on reset from PL power-on to PL ready to configure with POR override (2 ms maximum ramp rate).	15	15	15	15	15	ms, Max
		5	5	5	5	5	ms, Min
$T_{PS\_PROG\_B}$	PL program pulse width.	250	250	250	250	250	ns, Min
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	200	200	200	150	150	MHz, Max
DNA Port Switching							
F_{DNACK}	DNA port frequency (DNA_PORT).	200	200	200	175	175	MHz, Max
STARTUPE3 Ports							
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50.00	50.00	50.00	50.00	50.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	4	ms, Max

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